

PCI Express Card Electromechanical Specification

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June 9, 2021



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PCI Express Card Electromechanical Specification

Revision	Revision History	Date
1.0	Initial release.	7/22/2002
1.0a	Incorporated WG Errata C1-C7 and E1.	4/15/2003
1.1	Incorporated approved Errata and ECNs.	3/28/2005
2.0	Added support for 5.0 GT/s data rate.	4/11/2007
3.0	<ul style="list-style-type: none"> Added support for 8.0 GT/s data rate and incorporated approved Errata and ECNs. Incorporated the <i>PCI Express x16 Graphics 150W-ATX Specification</i> and the <i>PCI Express 225 W/300 W High Power Card Electromechanical Specification</i>. Re-imported all figures Updated Figure 6-1 and Figure 6-3 Fixed text notes in Chapter 6 and 9 Figures (took notes out of Illustrator and made them part of the Word file) Changed 306.67 MAX dimension to 326.03 MIN in Figure 9-3 	7/21/2013
4.0	<ul style="list-style-type: none"> Added support for 16.0 GT/s data rate and incorporated approved Errata and ECNs. Significant PCB layout updates to support signal integrity 	10/11/2013
4.0 r 0.7	Incorporated the following: <ul style="list-style-type: none"> CEM Comment tracking for 0.7 rev of 4.0 sent 2018 Feb 14, comments updated 03 March: 10.12.2017 - Cisco Comments on v0.7 r4.0 CEM, 10.02.2017 draft PCIe3 0_CEM_Embedding_Issue_Comm_Rev1_0 Incorporated new drawings CEM Comment tracking for 0.7 rev of 4.0 sent 2018 Feb 14, comments updated 03 March Wig	03/22/2018
4.0, 0.9	<ul style="list-style-type: none"> Updated drawings for clarity Miscellaneous text changes Incorporated AMD comments 	07/10/2019
4.0, 1.0	<ul style="list-style-type: none"> Replaced Figure 11-3, Figure 11-9, and Figure 11-36 Added Section 2.1.3, Clock Architecture Requirements Added Table 2-1. Clocking Architecture Requirements and Table 2-2. Common Clock Architecture Details Updated Acknowledgements section Release Candidate	08072019

5.0, 1.0	<p>Added support for 600 W, -48 N PCB geometry</p> <ul style="list-style-type: none"> • Updated Figure 3-1 • Added Section 6.3.6 • Added Chapter 10, <i>PCI Express 48VHPWR Auxiliary Power Connector Definition</i> • Added Chapter 9, <i>PCI Express 12VHPWR Auxiliary Power Connector Definition</i> • Replaced Sections 11.2 and 11.3.2 • Incorporated Manufacturer Test Mode Pin ECN • Added • Added Section B.3, 32 GT/s Test Channels • Incorporated C_{in} Maximum Increase ECN. • Replaced Figure 3-1, Figure 6-5, Dimension Tolerance, unless otherwise specified is: X.X = ± 0.25 mm, X.XX = ± 0.20 mm • Figure 9-4, Figure 11 40, Figure 11-22, Figure 11 43, and Figure 11 44. • Updated Table 5-3, Table 5-4, Table 5-7, and Table 5-8 • Added Table 5-9 • Added Section 5.3, <i>Optional Sideband Signal</i> • Removed reference to the <i>PCI Express Mini Card Electromechanical Specification</i> for CLKREQ# signal details • Added Section 2.8, CLKREQ# Signal (Optional) • Updated Table 2-6 • Updated Liquid Cooling Enablement section • Updated Figure 9-1 through Figure 9-8 • Update Figure 6-10 and Figure 6-11 • Replaced Figure 11-2 • Created Appendix D, Thermal Management • Moved Chapter 12 into Appendix D • Updated Appendix E, Acknowledgements • Misc updates 	June 9, 2021
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1. Introduction

This Card Electromechanical (CEM) specification is a companion for the *PCI Express® Base Specification, Revision 5.0*. Its primary focus is the implementation of an evolutionary strategy with earlier PCI™ desktop/server mechanical and electrical specifications.

This specification provides additional capabilities for PCI Express® (PCIe) Add-in Cards (AIC) within the existing framework of legacy system board form factors such as AGP and PCI. The PCI Express solution space was historically confined to Advanced Technology eXtended (ATX) or ATX-based form factors but is now integrated into a broader range of applications. The *Balanced Technology Extended (BTX) Interface Specification* is acknowledged as another form factor. Other connector and form factors that use PCI Express® signaling, are addressed in separate specifications.

This specification addresses signaling, power delivery and thermal management for individual Add-in Cards. Broader, chassis-level thermal and power management requirements stemming from the presence of multiple high-power Add-in Cards in a single chassis are beyond the scope of this specification.

The targeted applications for this specification extend well beyond the scope of the PCI Express 1.0 specification. Simple graphics cards and I/O adapters have given way to powerful coprocessors and accelerators. PCIe continues to provide an effective doubling of data rate with each generation. Over time, the advances in speed and capability, bring increased Add-in Card power and thermal demands. This specification addresses the delivery of increased electrical power to a PCI Express Add-in Card and provides increased card component and clearance volume for the management of thermals.

This specification continues to support multiple distinct maximum power levels for Add-in Cards: 10 W, 25 W, 75 W, 150 W, 225 W, and 300 W. In addition, this specification adds support for 600 W as the highest supported power. This specification recognizes that high power applications are no longer confined to graphics cards, and can include compute intensive network processing, GPUs, and machine learning cards, for example.

This specification introduces a 48 V Auxiliary Power rail and new power connectors supporting 600 W power delivery on a single 48 V or 12 V Auxiliary Power wire-to-board (WTB) connector.

This specification does not support the optional Hot Plug functionality for Add-in Cards beyond 75 W, but it does not preclude such support using an implementation-specific method. Starting with Revision 5.0 of this specification, it does not support unmanaged or surprise Hot Plug. It only supports managed Hot Plug for Add-in Cards up to 75W.

1.1. Terms and Definitions

x1, x2, x4, x8, x12, x16	x1 refers to one PCI Express Lane of basic bandwidth. For example: x4 refers to a collection of four PCI Express Lanes and is typically read as <i>by four</i> .
Add-in Card	A card that is plugged into a connector and mounted in a chassis slot.
AIC	Add-in Card.
AGP	Accelerated Graphics Port, card legacy form factor that predates PCI Express.
ATX	Advanced Technology eXtended, a system board form factor. Refer to the <i>ATX Specification</i> .
ATX-based form factor	Refers to the form factor that does not exactly conform to the ATX specification, but uses the key features of ATX, such as the slot spacing, I/O panel definition, etc.
Auxiliary power connector	An Add-in Card connector, other than the CEM slot connector, through which the Add-in Card receives a power rail. This specification defines these types of such connectors: 2x3 connector; 2x4 connector, 48VHPWR, and 12VHPWR.
Auxiliary signals	Signals, some of which are defined in the <i>PCI Express Base Specification</i> , that are used in conjunction with PCI Express signaling. Some are necessary for basic PCI Express operation (e.g., reference clock and reset) while others provide ancillary capabilities (e.g., the SMBus signals). See also Sideband signaling.
Basic bandwidth	The signal capacity of a single PCI Express Lane. (e.g. 32.0 GT/s for one PCI Express 5.0 Tx and one Rx differential pair).
Card	An Add-in Card that is plugged into a connector and mounted in a chassis slot.
Card Interoperability	Ability to operate with a PCI Express card plugged into different Link width connectors, for example, plugging a x1 card into a x16 slot.
CEM	Card Electromechanical.
Down-plugging	Plugging a larger Link mechanical width card into a smaller Link mechanical width connector, for example, plugging a x4 card into a x1 connector. (Support for down-plugging is outside the scope of this specification).
DUAL-SLOT Card	A card that plugs into a single edge connector – but whose volume occupies a total of two adjacent expansion slots.
ECN	Engineering Change Notice.
Evolutionary strategy	A strategy to develop the PCI Express connector and card form factors within today's chassis and system board form factor infrastructure constraints.
High bandwidth	Supports a larger number of PCI Express Lanes, such as a x16 card or connector.

Host	Typically, the motherboard or baseboard mounting the CEM Slot Connector. A riser card and connector are considered part of the host, by extension.
Hot Plug	Hot insertion and/or hot removal of a card into an active backplane or system board as defined in <i>PCI Express Base Specification</i> .
Hot swap	Insertion and/or removal of a card into a passive backplane. The card must satisfy specific requirements to support hot swap.
Lane	A differential Tx and Rx pair carrying PCI Express high-speed data.
Link	A collection of one or more PCI Express Lanes.
Low profile card	An Add-in Card whose height is no more than 68.90 mm (2.713 inches).
Managed Hot Plug	Add-in Card insertion or removal (Hot Plug) with explicit advanced chassis or Host level slot power switching to ensure card insertion and removal in an unpowered slot. Managed Hot Plug has no reliance on “first-break” connector contacts.
microATX	An ATX-based system board form factor. Refer to the <i>microATX Motherboard Interface Specification</i> .
OBFF	Optimized Buffer Flush/Fill.
PCIe	PCI Express.
PCI Express Connector	The card edge connector that accepts the CEM Add-in Card, typically mounted on the Host board or a riser card.
REFCLK	The reference clock differential pair consisting of auxiliary signals REFCLK+ and REFCLK-.
Riser	A PCB that mounts PCI Express CEM Slot Connectors and permits one or more Add-in Cards to connect to the Host through a single, separate connector.
Sentry Via	Additional ground via located adjacent to Auxiliary and Reserved signal pins in the through-hole connector footprint, intended to improve signal integrity.
SINGLE-SLOT Card	A card that uses a single expansion slot.
Sideband signaling	A method for signaling events and conditions using physical signals separate from signals forming the Link between two components. See also auxiliary signals.
Standard height card	An Add-in Card whose maximum height is no more than 111.28 mm (4.381 inches).
TIM	Thermal Interface Materials
TRIPLE-SLOT Card	A card that plugs into a single edge connector – but whose volume occupies a total of three adjacent expansion slots.
TTP	Thermal Transfer Plate

Unmanaged Hot Plug	Add-in Card insertion or removal (Hot Plug) that relies on shorter “first-break” connector contacts to trigger slot power switching at a chassis or Host level, to ensure card removal in an unpowered slot. Unmanaged Hot Plug is not permitted in the 5.0 Revision
Up-plugging	Plugging a smaller Link mechanical width card into a larger Link mechanical width connector, for example, plugging a x1 card into a x4 connector.
Wakeup	A mechanism used by a component to request the reapplication of main power when in the L2 Link state. Two such mechanisms are defined in the <i>PCI Express Base Specification</i> : Beacon and WAKE#. This specification requires the use of WAKE# on any Add-in Card or system board that supports wakeup functionality.

1.2. Reference Documents

This specification references the following documents:

- *PCI Express Base Specification*, Revision 5.0
- *PCI Local Bus Specification*, Revision 3.0
- *PCI Express Jitter Modeling*
- *PCI Express Jitter and BER*
- *Combined Power ECN to PCI Express Base 5.0 Specification*
- *ASME Y14.5-2009 Dimensioning and Tolerancing*
- *ATX Specification*, Revision 2.2
- *microATX Motherboard Interface Specification*, Revision 1.2
- *SMBus Specification*, Revision 3.1
- *IEEE Standard 1149.1, Test Access Port and Boundary Scan Architecture*
- *Compact PCI Hot-swap Specification*
- *EIA-364-1000.01: Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications*
- *EIA-364: Electrical Connector/Socket Test Procedures Including Environmental Classifications*
- *ISO 3744, Acoustics – Determination of Sound Power Levels of Noise Sources Using Sound Pressure – Engineering Method in an Essentially Free Field Over a Reflecting Plane*
- *ISO 7779, Acoustics – Measurement of Airborne Noise Emitted by Information Technology and Telecommunications Equipment*
- *PCI Express Label Specification and Usage Guidelines*, Revision 1.1
- *PCI Express Architecture PHY Test Specification*, Revision 5.0 for PCI Express Architecture
- *Balanced Technology Extended (BTX) Interface Specification*, Revision 1.0b
- *PCI Express Graphics Card Thermal Mechanical Design Guidelines*
- *EIA 364-101 – Attenuation Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection Systems*
- *EIA 364-90 – Crosstalk Ratio Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection Systems*
- *EIA 364-108 – Impedance, Reflection Coefficient, Return Loss, and VSWR Measured in the Time and Frequency Domain Test Procedure for Electrical Connectors, Sockets, Cable Assemblies, or Interconnection Systems*

- *PCI Express Connector High Speed Electrical Test Procedure*

1.3. Specification Contents

This specification contains the following information:

- Auxiliary signals
- Add-in Card hot insertion and hot removal
- Power delivery
- Thermal management
- Add-in Card electrical budget
- Connector specification
- Card form factors and implementation
- System requirements
- Supplemental auxiliary power connector specification

1.4. Objectives

The objectives of this specification are:

- Support 32.0 GT/s, 16.0 GT/s, 8.0 GT/s, 5.0 GT/s and 2.5 GT/s data rate (per direction)
- Enable Managed Hot Plug and hot swap where they are needed
- Leverage desktop and server commonality
- Allow co-existence of both PCI and PCI Express Add-in Cards
- Forward looking for future scalability
- Extensible for future bandwidth needs
- Allows future evolution of PC architecture
- Maximize card interoperability for user flexibility
- Low cost
- Support for PCI Express Add-in Cards that have higher power requirements
- Upgradeability
- Enhanced end user experience

1.5. Electrical Overview

The electrical part of this specification addresses auxiliary signals, hot insertion and hot removal (Hot Plug), power delivery, and Add-in Card interconnect electrical budgets. The PCI Express Transmitter and Receiver electrical requirements are specified in the *PCI Express Base Specification*.

Besides the signals that are required to transmit/receive data via the PCI Express interface, there are also signals that may be necessary to implement the PCI Express interface in a system environment, or to provide certain desired functions. These signals are referred to as the auxiliary signals. They include:

- Reference clock (REFCLK-/REFCLK+), must be supplied by the system (see Section 2.1)
- Add-in Card presence detect pins (PRSNT1# and PRSNT2#), required
- PERST#, required
- CLKREQ#, optional
- JTAG, optional
- SMBus, optional
- Wake (WAKE#), required only if the device/system supports wakeup and/or the Optimized Buffer Flush/Fill (OBFF) mechanism
- Power Brake (PWRBRK#), optional

- +3.3 Vaux, optional, required if device/system supports SMBus.

REFCLK, CLKREQ#, JTAG, SMBus, PERST#, WAKE# and PWRBRK# are described in Chapter 2; +3.3Vaux is described in Chapter 4; and PRSNT1# and PRSNT2# are described in Chapter 3.

Both managed Hot Plug and hot swap of PCI Express Add-in Cards are supported, but their implementation is optional. Hot swap is supported with other form factors and will be described in other specifications.

Presence detect pins (PRSNT1# and PRSNT2#) are located in each end of the connectors and Add-in Cards and are the same length as the rest of the pins.

Starting with Revision 5.0 of this specification, the presence detect card edge fingers are the same length as all other card edge fingers. As a result, this specification does not support unmanaged hot plug. Electrical support for Managed Hot Plug continues in this specification. Hot Plug is still required in the *PCI Express Base Specification*.

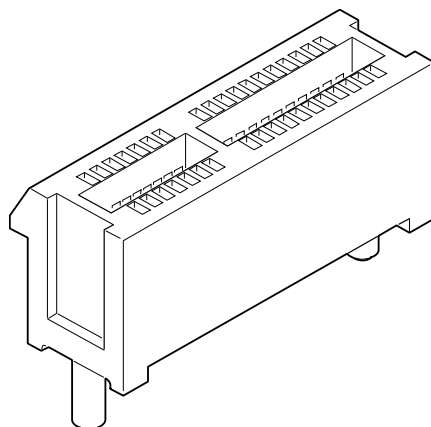
To support Hot Plug, presence detect pins (PRSNT1# and PRSNT2#) are defined in each end of the connectors and Add-in Cards. Chapter 3 discusses the detailed implementation of PCI Express Hot Plug.

Chapter 4 specifies the PCI Express Add-in Card electrical requirements, which include power delivery and interconnect electrical budgets. Power is delivered to the PCI Express Add-in Cards via PCI Express connectors, using three voltage rails: +3.3V, +3.3Vaux, and +12V. The +3.3 Vaux voltage rail is not required for all platforms (refer to Section 4.1 for more information on the required usage of 3.3 Vaux). The maximum Add-in Card power definitions are based on the card size and Link widths (described in Section 4.2). Chapter 4 describes the interconnect electrical budgets, focusing on the Add-in Card loss and jitter requirements. Chapter 5 describes optional power delivery to Add-in Cards via Auxiliary Power connectors.

1.6. Mechanical Overview

PCI Express is used in many different applications in desktop, mobile, server, as well as networking and communication equipment. Consequently, multiple variations of form factors and connectors will exist to suit the unique needs of these different applications.

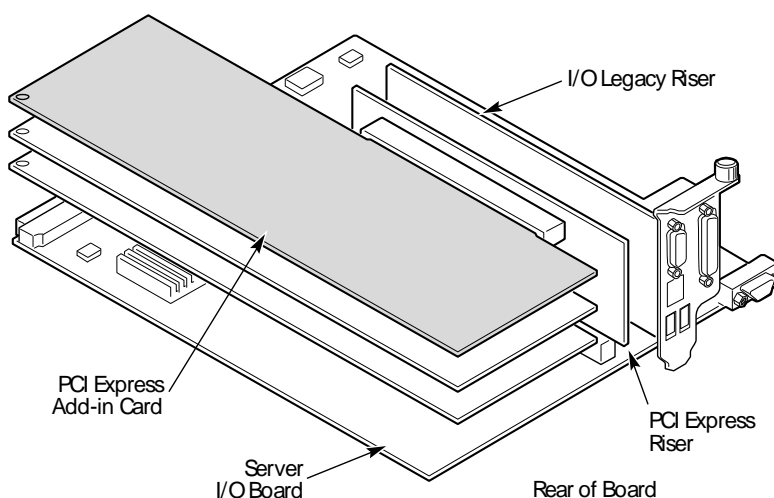
Figure 1-1 shows an example of the vertical edge-card PCI Express connector to be used in ATX or ATX-based systems. There is a family of such connectors, containing one to 16 PCI Express Lanes. The basic bandwidth (BW) version supports a single PCI Express Lane. The high bandwidth version supports 16 PCI Express Lanes and is used for applications that require higher bandwidth, such as graphics, high-speed networking, or compute accelerators.



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Figure 1-1: Vertical Edge-Card Connector

Vertical edge card connectors also have applications in the server market segment. Figure 1-2 shows an example of a server configuration using a PCI Express riser card. A riser is typically considered to be part of the System Board, in terms of delineating Add-in Cards and System Boards,



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Figure 1-2: Example Server I/O Board with PCI Express Slots on a Riser

This specification focuses on the vertical edge card PCI Express connectors and form factor requirements by covering the following:

- Connector mating interfaces and footprints for through-hole and surface mount technologies.
- Electrical, mechanical, and reliability requirements of the connectors, including the connector testing procedures.
- Add-in Card form factors – including their keepout areas within the card as well as the keepout areas required to exit the chassis including the I/O connectors and mating cables for a typical desktop system chassis (ATX/microATX form factor). Connector and Add-in Card locations, as well as keepouts on a typical desktop system board (ATX/microATX form factor).

Connector definitions and requirements are addressed in Chapter 6 and Add-in Card form factors and implementation issues are discussed in Chapter 11.

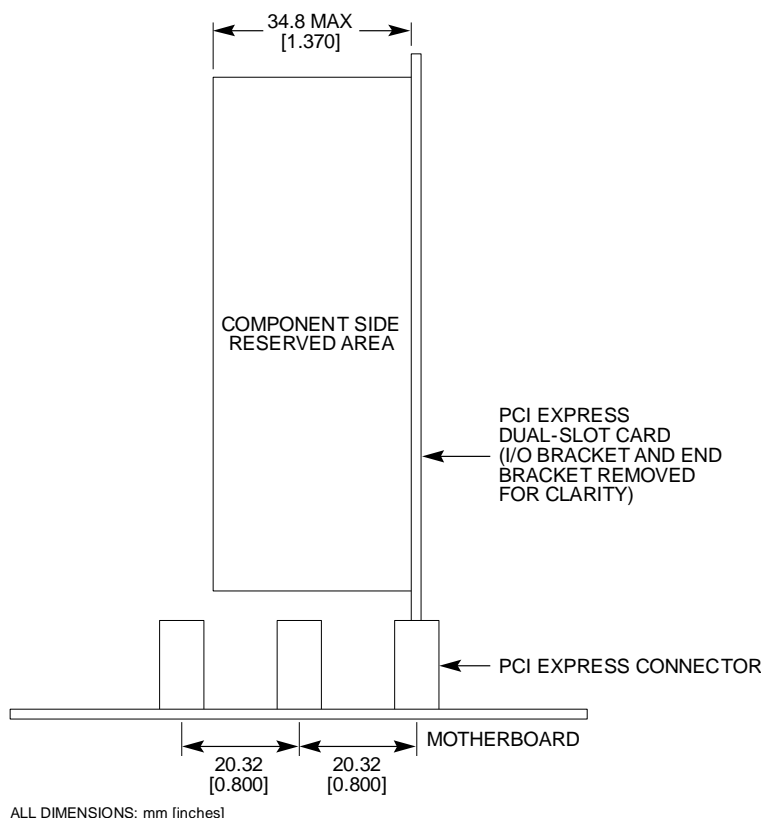
- In the figures throughout this document, driving dimensions are mm. Inch dimensions are shown for convenience.
- In all Card Assembly drawings throughout this specification:
 - a. Datum V is the Primary Component Side of the Card Assembly.
 - b. Datum W is the leading surface of the edge connector.
 - c. Datum X is the midplane of the two parallel planes made perpendicular to Datum V and Datum W on the measured surfaces of the slot sides.

1.7. 150 W Overview

A PCI Express 150 W Add-in Card is defined as a card that consumes greater than 75 W and up to 150 W inclusive. A card that uses a single expansion slot is described as a SINGLE-SLOT Add-in Card. A card that extends into the adjacent expansion slot is described as a DUAL-SLOT Add-in Card. A card that extends into the two adjacent expansion slots is described as a TRIPLE-SLOT Add-in Card. A 150 W Add-in Card, as with any CEM Add-in Card, may be SINGLE-SLOT, DUAL-SLOT, or TRIPLE-SLOT. A system that supports a PCI Express 150 W Add-in Card is required to ensure that sufficient power and thermal support exists. For example, in an ATX form factor system, the adjacent expansion slot can be vacant, allowing for 1.37 inches of clearance for the Add-in Card (illustrated in Figure 1-3) to support a 150 W or lower power DUAL-SLOT Add-in Card.

The DUAL-SLOT Add-in Card plugs into the standard PCI Express connector but is not permitted to plug into any other adjacent Add-in Card connectors for any purpose.

The PCI Express 150 W Add-in Card draws a maximum of 75 W from the standard PCI Express Slot connector. Additional power, up to 75 W, is provided through an additional auxiliary connector that is detailed in this specification. Therefore, the maximum power that must be provided to a PCI Express 150 W Add-in Card is 150 W.



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Figure 1-3: Example Orientation for DUAL-SLOT Add-in Cards

1.8. 225 W and 300 W Add-in Card Overview

A PCI Express 225 W Add-in Card is defined as a card that exceeds PCI Express 150 W power delivery or thermal capability and, as such, consumes greater than 150 W with support for up to 225 W inclusive. This card, as with any CEM Add-in Card, may be a SINGLE-SLOT, DUAL-SLOT, or TRIPLE-SLOT Add-in Card. A system that supports a PCI Express 225 W Add-in Card is required to ensure that sufficient power and thermal support exists. For example, in an ATX system, the adjacent expansion slot may be left vacant allowing for 34.8 mm (1.37 inches) maximum clearance for the Add-in Card, as illustrated in Figure 1-3. The area on the Add-in Card that utilizes this height, as well as the restricted height of the secondary side, is determined by the general PCI Express Add-in Card requirements for these dimensions.

A PCI Express 300 W Add-in Card is defined as a card that consumes greater than 225 W with support for up to 300 W inclusive. This card, as with any CEM Add-in Card, may be a SINGLE-SLOT, DUAL-SLOT, or TRIPLE-SLOT Add-in Card. A system that supports a PCI Express 300 W Add-in Card is required to ensure that sufficient power and thermal support exists. As another example, in an ATX form factor system, the adjacent two expansion slots may be left vacant allowing for 55.12 mm (2.17 inches) maximum clearance for the Add-in Card, as illustrated in Figure 1-4. The area on the Add-in Card that utilizes this height, as well as the restricted height of the secondary side, is determined by the general PCI Express Add-in Card requirements for these dimensions.

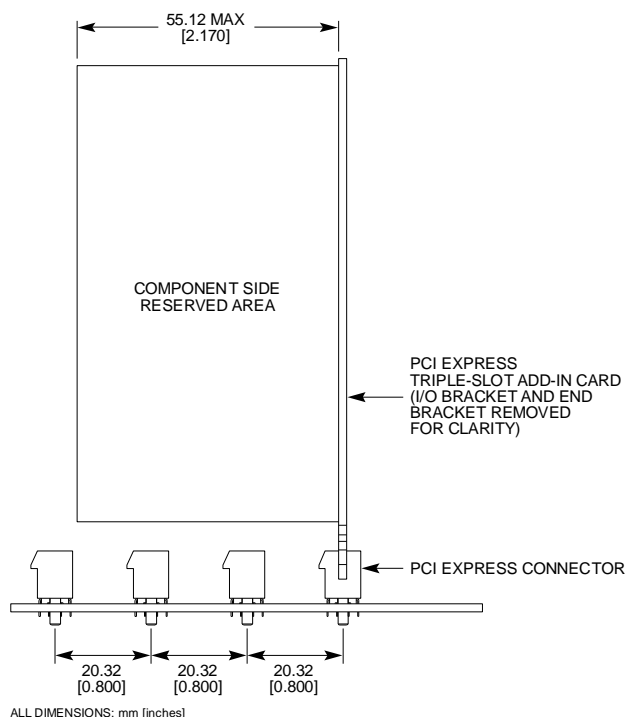


Figure 1-4: Example Orientation for TRIPLE-SLOT Cards

The PCI Express 225 W/300 W Add-in Card draws a maximum of 75 W through the PCI Express Connector. Additional power, up to 150 W for the 225 W Add-in Card and up to 225 W for the 300 W Add-in Card, is provided through additional auxiliary connector(s) that is(are) detailed in this specification.

1.9. 600 W Add-in Card Overview

A PCI Express 600 W Add-in Card is defined as a card that consumes greater than 300 W with support for up to 600 W inclusive. This card, as with any CEM Add-in Card, may be a SINGLE-SLOT, DUAL-SLOT, or TRIPLE-SLOT Add-in Card. A system that supports a PCI Express 600 W Add-in Card is required to ensure that enough power and thermal support exists. A 600 W card must be designed to draw no more than 600 W total from any combination of the power connectors. The PCI Express 600 W Add-in Card can draw a maximum of 75 W through the PCI Express Connector. It can draw a maximum of 600 W from the Auxiliary Power connectors alone, but it must manage power consumption to ensure that the combined total draw from Slot Power and Auxiliary Power does not exceed 600 W.

2. Auxiliary Signals

The auxiliary signals are provided on the connector to assist with certain system-level functionality or implementation. The high-speed signal voltage levels are compatible with advanced silicon processes. The optional low speed signals are defined to use the +3.3V or +3.3Vaux supplies, as they are the lowest common voltage available. Most ASIC processes have high voltage (thick gate oxide) I/O transistors compatible with +3.3 V. Use of the +3.3 V supply allows PCI Express signaling to be used with existing control bus structures, avoiding a buffered set of signals and bridges between the buses.

The PCI Express Slot connector and Add-in Card interfaces support the following auxiliary signals:

- **REFCLK-/REFCLK+** (required) are low voltage differential signals. Requirements for REFCLK for a system are defined in *PCI Express Base Specification*. A system board must provide a reference clock that meets all requirements for the common clock architecture defined for the reference clock in the *PCI Express Base Specification* and all the requirements defined in this specification.
- **PERST#** (required) indicates when the applied main power is within the specified tolerance and stable. PERST# goes inactive after a delay of T_{PVPERL} time from the power rails achieving specified tolerance on power up.
- **WAKE#** (optional) is an open-drain, active low signal that is driven low by a PCI Express function to re-activate the PCI Express Link hierarchy's main power rails and reference clocks. It is required on any Add-in Card or system board that supports wakeup functionality compliant with this specification. WAKE# is also used by the system to signal to the PCI Express function in conjunction with the Optimized Buffer Flush/Fill (OBFF) mechanism.
- **SMBCLK** (optional) is the SMBus interface clock signal. It is an open-drain signal.
- **SMBDAT** (optional) is the SMBus interface address/data signal. It is an open-drain signal.
- **JTAG** (TRST#, TCK, TDI, TDO, and TMS) (optional) are the pins to support IEEE Standard 1149.1. They are included as an optional interface for PCI Express devices. IEEE Standard 1149.1 specifies the rules and permissions for designing an 1149.1-compliant IC.
- **PRSNT1#** (required) signal is an Add-in Card presence detect pin. See Chapter 3 for a detailed description.
- **PRSNT2#** (required) signal is an Add-in Card presence detect pin. See Chapter 3 for a detailed description.
- **CLKREQ#** (optional) signal is an open drain, active low signal that is driven low by the card to request that the PCI Express reference clock be available (active clock state) to allow the PCI Express interface to send/receive data. See Section 2.8 in this specification for details on the functional and electrical requirements for the CLKREQ# signal. The CLKREQ# signal is used by the optional L1 PM Substates mechanism. In this case, CLKREQ# is asserted by either the system or Add-in Card to initiate an L1 exit. Refer to the *PCI Express Base Specification* for details on the functional requirements for the CLKREQ# signal when implementing L1 PM Substates.
- **PWRBRK#** (optional) is an open-drain, active low signal that is driven low by the system to signal an Emergency Power Reduction mechanism.
- **RSVD** (Reserved) must not be used for any purpose.
- **MFG (optional)** is a manufacturer test mode signal. Pin functionality is defined by the Add-in Card (AIC) manufacturer and must be disabled in non-manufacturing environments.

All Add-in Card edge-fingers that are assigned to auxiliary signals among pins A12/B12 through A82/B82 must be both present and terminated even if their electrical functions are not implemented, as described in Section 11.2.2 and 11.2.5. This applies to the pin positions for PWRBRK#, RSVD, MFG, CLKREQ#, and all PRSNT2# edge-finger contacts.

The SMBus interface pins are collectively optional for both the Add-in Card and the system board. If the optional management features are implemented, SMBCLK and SMBDAT are both required. Similarly, the JTAG pins are collectively optional. If this test mode is implemented, all the JTAG pins are required. For additional system requirements related to these signals refer to the *PCI Local Bus Specification*.

2.1. Reference Clock

2.1.1. Low Voltage Swing, Differential Clocks

To reduce jitter and allow for future silicon fabrication process changes, low voltage swing, differential clocks are used, as illustrated in Figure 2-1. Requirements for REFCLK are defined in the *PCI Express Base Specification*.

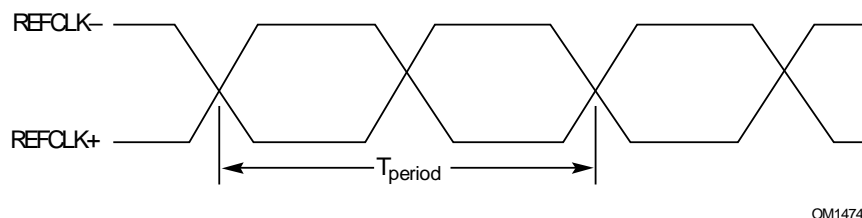
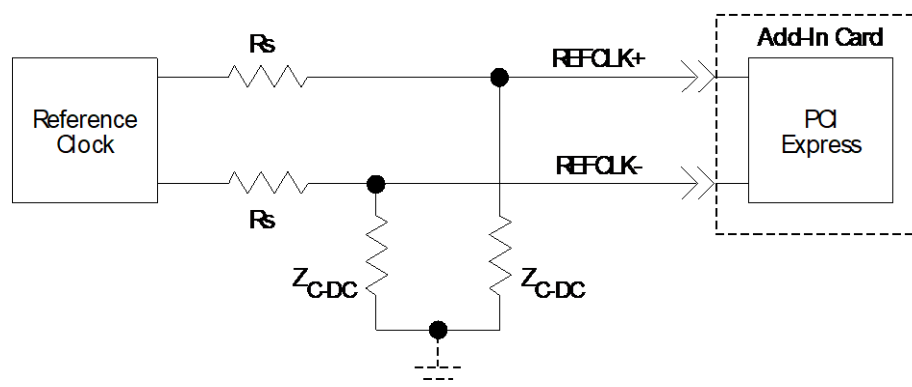


Figure 2-1: Differential REFCLK Waveform

The reference clock pair is routed point-to-point to each connector from the system board per best-known clock routing rules. The reference clock distribution to all devices must be matched to within 15 inches on the system board. The transport delay delta between the data and clock at the Receiver must be less than 12 ns. The combination of the maximum reference clock mismatch and the maximum channel length will contribute approximately 9-10 ns and the remaining time is allocated to the difference in the insertion delays of the Tx and Rx devices. The routing of each signal in any given clock pair between the clock source and the connector must be well matched in length (< 0.005 inch) and appropriately spaced away from other non-clock signals to avoid excessive crosstalk.

The system board must provide any terminations required by the clock source. An example termination topology for a current-mode clock generator is shown in Figure 2-2. EMI emissions will be reduced if clocks to open sockets are shut down at the clock source. The method for detecting the presence of a card in a slot and controlling the clock gating is platform specific and is not covered in this specification.



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Figure 2-2: Example Current Mode Reference Clock Source Termination

Termination on the Add-in Card using discrete components on the PCB is allowed and is not covered by the specifications in Section 2.1.3. While the same measurement techniques can be used as specified in that section, Receiver termination will reduce the nominal swing and rise and fall times by half. The low input swing and low slew rates need to be validated against the clock Receiver requirements as they can cause excessive jitter in some clock input buffer designs.

The reference clock timings are based on nominal 100 Ω , differential pair routing with approximately 0.127 mm (5 mil) trace widths. This timing budget allows for a maximum Add-in Card trace length of 4.0 inches. No specific trace geometry, however, is explicitly defined in this specification.

2.1.2. Spread Spectrum Clocking (SSC)

The reference clocks may support spread spectrum clocking. Any given system design may or may not use this feature contingent on platform-level timing requirements. The requirements for spread spectrum modulation rate and magnitude are given in the *PCI Express Base Specification*.

2.1.3. Clock Architecture Requirements

The CEM 5.0 connector supports following clocking architectures:

- Common Clock
- SRIS/SRNS (only allowed for bridging to other form-factors for example via CEM 5.0 risers)

Table 2-1 summarizes the supported clocking architectures for various CEM 5.0 components.

Table 2-1. Clocking Architecture Requirements

Clock Architecture	CEM 5.0 Platform	PCIe 5.0 CEM Add-in Card	CEM 5.0 Riser	PCIe 5.0 Retimer
Common Clock	Required	Required	Optional	Required
SRIS	Not Allowed	Not Allowed	Optional	Optional
SRNS	Not Allowed	Not Allowed	Optional	Optional

For CEM 5.0 Platforms and Add-in Cards, common clock is the required clocking architecture. Separate reference clock architectures (SRIS/SRNS) are not CEM compliant.

- CEM 5.0 compliant host platform is required to supply reference clock to the connector.
- CEM 5.0 compliant Add-in Card is required to use the reference clock supplied at the connector.

CEM 5.0 riser implementations have an option to choose either common clock or separate reference clock architectures. The clocking flexibility in riser implementations is allowed to bridge to other form-factors.

PCIe 5.0 Retimers are required to support common clock architecture and are optionally allowed to support SRIS/SRNS.

Table 2-2 shows clocking details when supporting Common Clock Architecture.

- CEM 5.0 compliant host platforms are required to source the clock to the Add-in Cards.
- CEM 5.0 Add-in Cards are not allowed to source the clock.
- Reference clock SSC implementation is optional for CEM 5.0 host platforms.
- CLKREQ# implementation is optional for CEM 5.0 platforms and Add-in Cards, depending on whether L1-PM sub-states are supported and/or whether clock power management is supported.
- Depending on implementation, CEM 5.0 Risers and Retimers are allowed to source clock to the downstream component.

Table 2-2. Common Clock Architecture Details

Common Clock Details	CEM 5.0 Platform	PCIe 5.0 CEM Add-in Card	CEM 5.0 Riser	PCIe 5.0 Retimer
Clock Source	Required	Not Allowed	Optional	Optional
SSC	Optional	N/A	Optional	Optional
CLKREQ#	Optional	Optional	Optional	Optional

2.1.4. REFCLK AC Specifications

REFCLK must meet the requirements defined in the *PCI Express Base Specification*.

2.1.5. REF CLK Phase Jitter Specification

The phase jitter specification and measurement methodology are discussed in the *PCI Express Base Specification*.

To account for phase jitter on the REFCLK, a dual-port methodology for simultaneously assessing the system board data and reference clock is described with specified limits in the following sections. This dual port methodology is applicable to 16 GT/s, 8 GT/s, and 5 GT/s. Dual-port methodology is not used for 2.5 GT/s and 32.0 GT/s.

2.1.6. REFCLK Phase Jitter Specification for 32.0 GT/s Systems

This specification details the requirements for measuring 100 MHz REFCLK for 32.0 GT/s capable systems using common clock architecture, at the card electromechanical connector. The phase jitter of the reference clock is to be measured using the behavioral CDR, TX and RX PLL functions specified in the PCI Express base Specification for 32.0 GT/s.

The maximum allowed magnitude of the reference clock RMS Rj is given in Table 2-3. The RMS Rj requirement in Table 2-3. must be met irrespective of REFCLK having Spread Spectrum Clocking (SSC) enabled or disabled.

Multiple methods can be used to measure the maximum allowed RMS Rj phase jitter value. Capture at least 160,000 clock intervals. (1.6 ms).

Table 2-3. Maximum Allowed Reference Clock RMS Rj Phase Jitter

Data Rate	Maximum Rj RMS (fs)
32 GT/s	200

Note: Reference clock value in this table is referenced to 100 Ohm differential load at the end of an isolated (no crosstalk) 100 Ω trace.

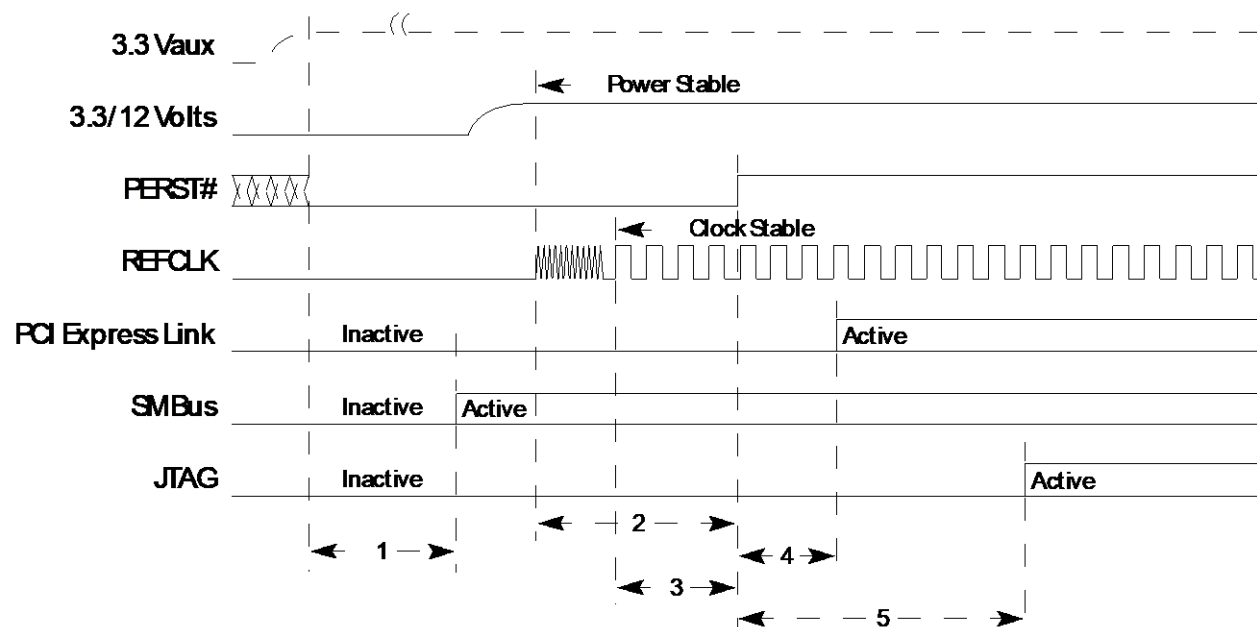
2.2. PERST# Signal

The PERST# signal is used to indicate when the power supply is within its specified voltage tolerance and is stable. It also initializes a component's state machines and other logic once power supplies stabilize. On power-up, the de-assertion of PERST# is delayed 100 ms (T_{PVPERL}) from the power rails achieving specified operating limits. Also, within this time, the reference clocks (REFCLK+, REFCLK-) also become stable, at least $T_{PERST-CLK}$ before PERST# is de-asserted. PERST# is asserted in advance of the power being switched off in a power-managed state like S3. PERST# is asserted when the power supply is powered down, but without the advanced warning of the transition.

2.2.1. Initial Power Up (G3 to S0)

While PERST# is active, all PCI Express functions on the Add-in Card are held in reset. This permits the main supplies to ramp up to their specified levels (+3.3 V and +12 V). During this stabilization time, the REFCLK starts and stabilizes. After there has been time (T_{PVPERL}) for the power and clock to become stable, PERST# is de-asserted and the PCI Express functions can exit reset.

On initial power-up, the hardware default state of the Active State Power Management Control field in the Link Control register must be set to 00b (see Figure 2-3). The state of this field may be changed by the system BIOS or the operating system. Other software agents must not change this field.



1. 3.3Vaux stable to SMBus driven (optional). If no 3.3Vaux on platform, the delay is from +3.3V stable
2. Minimum time from power rails within specified tolerance to PERST# inactive (T_{PVPERL})
3. Minimum clock valid to PERST# inactive ($T_{PERST-CLK}$)
4. Minimum PERST# inactive to PCI Expresslink out of electrical idle
5. Minimum PERST# inactive to JTAG driven (optional)

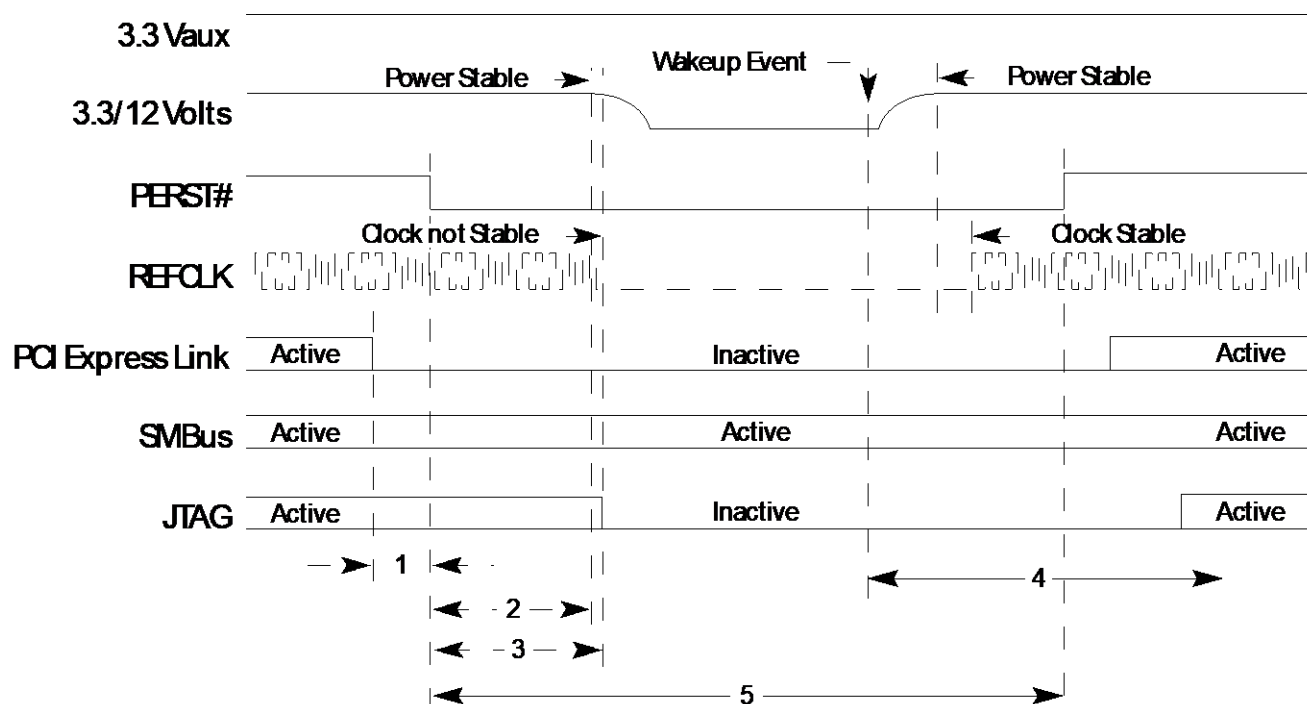
OM14742B

Figure 2-3: Power Up

2.2.2. Power Management States (S0 to S3/S4 to S0)

If the system wants to enter S3/S4, devices are placed into D3_{hot} states with Links in L2 prior to any power transitions at the slot. The main power and reference clock supplied to the PCI Express slot will go inactive and stay inactive until a wakeup event. Due to the removal of main power, devices enter the D3_{cold} state. During the D3_{cold} state, +3.3Vaux (if supplied) remains at +3.3 V. On the wakeup event, the power manager restores the main power and reference clocks. As in the last section, PERST# de-asserts T_{PVPERL} after the clock and power are stable.

On resume from a D3_{cold} state, the hardware default state of the Active State Power Management Control field in the Link Control register must be set to 00b. The state of this field may be changed by the system BIOS or the operating system. Other software agents must not change this field.



1. The PCI Express link will be put into electrical idle prior to PERST# going active.
2. PERST# goes active before the power on the connector is removed.
3. Clock and JTAG go inactive after PERST# goes active.
4. A wakeup event resumes the power to the connector, restarts the clock, and the sequence proceeds as in power up.
5. The minimum active time for PERST# is T_{PERST} .

OM14743I

Figure 2-4: Power Management States

2.2.3. Power Down

A power rail (+12V, +3.3V, or +3.3Vaux) is deemed to be valid or stable if the specified voltage is within the associated voltage tolerances defined in Table 4-1. Once a power rail is deemed stable, an invalid or unstable rail is defined as a rail that has dropped below the specified minimum voltage levels (e.g., below +3.00 V for the +3.3V rails). For purposes of detecting an out-of-tolerance power source, the threshold for detection must be established in a window range of no more than 500 mV below the specified minimum voltage level for the +3.3V and +3.3Vaux rails (i.e., +2.50 V) and +1.34 V below for the +12V rail (i.e., +9.70 V). Figure 2-5 illustrates these threshold windows. Figure 2-6 shows Power Down.

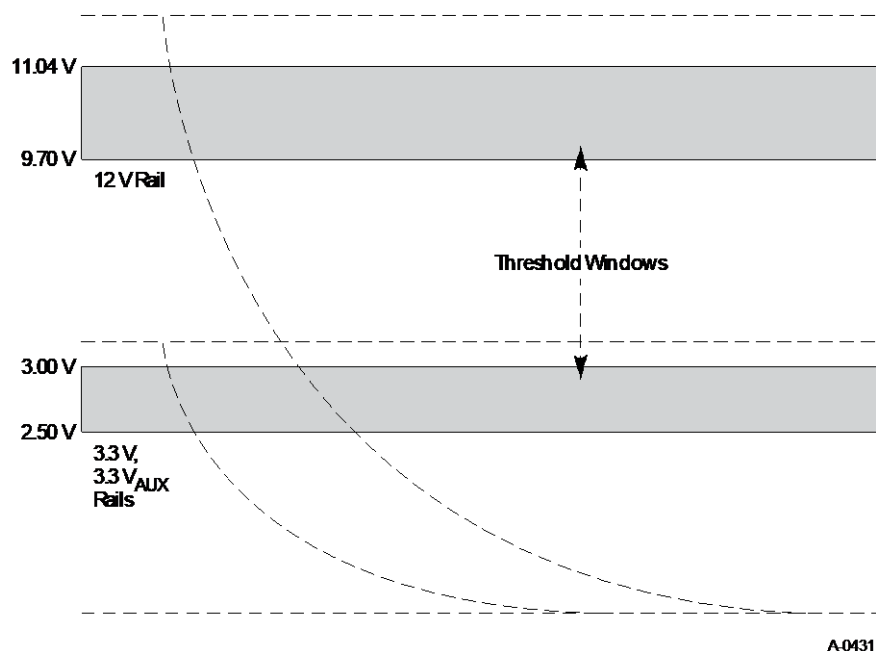
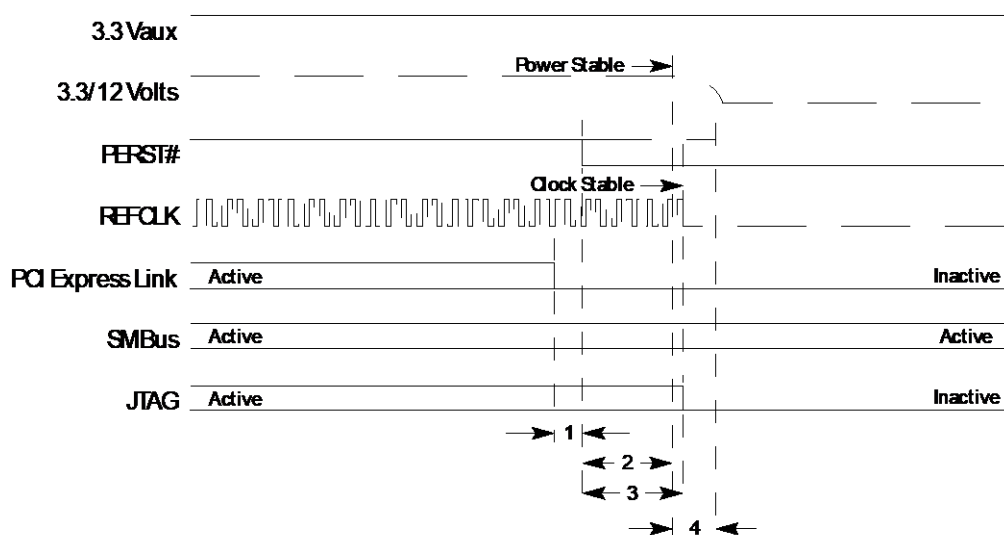


Figure 2-5: Out-of-tolerance Threshold Windows



1. The PCI Expresslink will be put into an inactive state (Device in D3_{hot}) prior to PERST# going active, except in the case of a surprise power down.
2. PERST# goes active before the power on the connector is removed.
3. Clock and JTAG go inactive after PERST# goes active.
4. In the case of a surprise power down, PERST# goes active T_{FAIL} after power is no longer stable.

OM14744I

Figure 2-6: Power Down

2.3. WAKE# Signal

The WAKE# signal is an open drain, active low signal that is driven low by a PCI Express Add-in Card to request the platform to reactivate the PCI Express slot's main power rails and reference clocks. The Downstream Ports also use the WAKE# signal to signal to functions on the Add-in Card in conjunction with the OBFF mechanism. Only Add-in Cards that support either the wake process or the OBFF mechanism connect to this pin. If the Add-in Card has wakeup capabilities, it must support the WAKE# function. Likewise, only systems that support the wakeup function or the OBFF mechanism need to connect to this pin. Such systems are not required to support Beacon as a wakeup mechanism but are encouraged to support it. If the wakeup process is used, the +3.3Vaux supply must be present and used for this function. The assertion and de-assertion of WAKE# are asynchronous to any system clock. (See the *PCI Express Base Specification*, for more details on PCI-compatible power management.)

If the WAKE# signal is supported by a slot, the signal is connected to the platform's power management (PM) controller. The WAKE# signal can either be bused to multiple PCI Express Add-in Card connectors forming a single input connection at the PM controller, or the individual connectors have individual connections to the PM controller. Hot Plug requires that the WAKE# signal is isolated between connectors and driven inactive during the hot insertion/hot removal events. See Section 6.1 for the WAKE# signal connector pin assignment.

3.3 V auxiliary power (+3.3Vaux) must be used by the asserting and receiving ends of the WAKE# signal to revive the hierarchy. The system vendor must also provide a pull-up on WAKE# with its bias voltage reference being supplied by the auxiliary power source in support of Link reactivation. The voltage that the system board uses to terminate the WAKE# signal can be lower than the auxiliary supply voltage to be compatible with lower voltage processes of the system PM controller. However, all potential drivers of the WAKE# signal must be +3.3 V tolerant.

The WAKE# signal is only asserted by the Add-in Card when all its functions are in the D3_{cold} state and at least one of its functions is enabled for wakeup generation (see the *PCI Express Base Specification* for details of enabling wakeup generation).

The WAKE# signal is not PME# and must not be attached to the PCI-PME# interrupt signals. WAKE# causes power to be restored but must not directly cause an interrupt.

If the PCI Express Add-in Card supports the OBFF mechanism defined in the *PCI Express Base Specification*, then the WAKE# signal may be used as an input to the Add-in Card. Refer to the *PCI Express Base Specification* for specifics of the OBFF mechanism.

WAKE# has additional electrical requirements over and above standard open drain signals that allow it to be shared between devices that are powered off and those that are powered on using auxiliary power for example. The additional requirements include careful circuit design to ensure that a voltage applied to the WAKE# signal network never causes damage to a component even if that particular component's power is not applied.

Additionally, the device must ensure that it does not pull WAKE# low unless WAKE# is being intentionally asserted in all cases, including when the related function is in D3_{cold}, or when the Add-in Card is being inserted or removed.

This means that any component implementing WAKE# must be designed such that:

- Unpowered WAKE# output circuits are not damaged if a voltage is applied to them from other powered “wire-ORed” sources of WAKE#.
- When power is removed from its WAKE# generation logic, the unpowered output does not present a low impedance path to ground or any other voltage.

These additional requirements ensure that the WAKE# signal network continues to function properly when a mixture of auxiliary powered and unpowered components have their WAKE# outputs wire-ORed together. Be aware that most commonly available open drain and tri-state buffer circuit designs used “as is” do not satisfy the additional circuit design requirements for WAKE#.

Other requirements on the system board/Add-in Card designs include:

- Common ground plane reference between slots/components attached to the same WAKE# signal.
- Split voltage power planes (+3.3Vaux vs. +3.3V) are required if +3.3Vaux is supplied to the connector(s).
- If +3.3Vaux is supplied to one PCI Express connector in a chassis, it must be supplied to all PCI Express connectors in that chassis.
- If WAKE# is supported on one PCI Express connector in a chassis, it must be supported on all PCI Express connectors in that chassis.
- If the system does not support +3.3Vaux, the +3.3Vaux connector pin is left open on the system board. See the *PCI Express Base Specification*, for +3.3Vaux power requirements.
- +3.3Vaux voltage supply may be present even if the device is not enabled for wakeup events.
- +3.3V at the PCI Express connector may be switched off by the system.

- Add-in Cards are permitted to generate the Beacon wakeup mechanism in addition to using the WAKE# mechanism, although the system is not required to provide support for Beacon.
- If the Add-in Card uses the Beacon mechanism in addition to the WAKE# mechanism, the Beacon may be ignored by the system. Circuits that support the wake function and are intended to work in any PCI Express system must be designed to generate the Beacon on their PCI Express data lines.

PCI Express Add-in Card designers must be aware of the special requirements that constrain WAKE# and ensure that Add-in Cards do not interfere with the proper operation of the WAKE# network. The WAKE# input into the system may de-assert as late as T_{WKRF} after the WAKE# output from the function de-asserts (i.e., the WAKE# pin must be considered indeterminate for several cycles after it has been de-asserted).

The value of the pull-up resistor for WAKE# on the system board must be derived taking into account the total possible capacitance on WAKE# to ensure that WAKE# charges up to a logic high voltage level in no more than 100 ns. (Refer to the *PCI Local Bus Specification*, for information on pull-up resistors.)



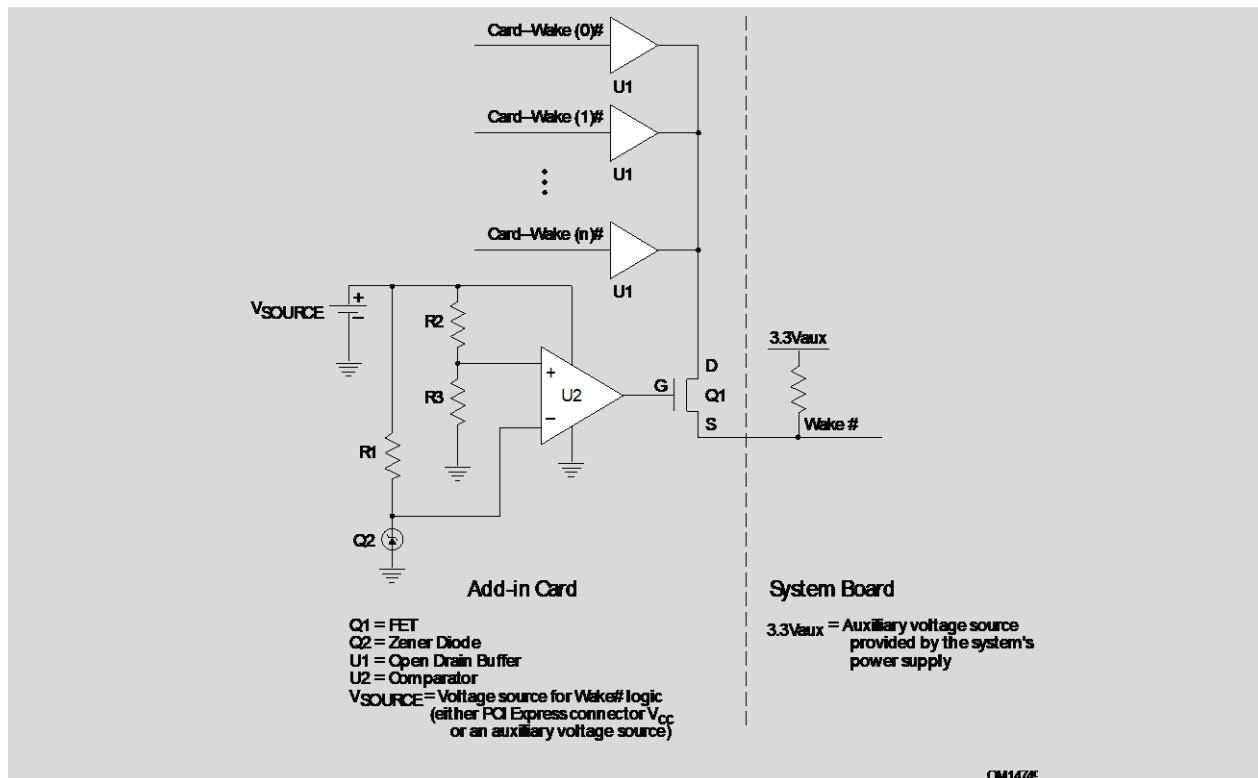
IMPLEMENTATION NOTE

Example WAKE# Circuit Design

The following diagram is an example of how the WAKE# generation logic could be implemented. In this example, multiple PCI Express functions have their WAKE# signals ganged together and connected to the single WAKE# pin on the PCI Express Add-in Card connector.

The circuit driving the gate of transistor Q1 is designed to isolate the Add-in Card's WAKE# network from that of the system board whenever its power source (V_{SOURCE}) is absent.

If the card supplies power to its WAKE# logic with the PCI Express connector's +3.3V supply (i.e., it does not support wakeup from D3_{cold}), then all WAKE# sources from the card will be isolated from the system board when the Add-in Card's +3.3V rail is switched off. Add-in Cards that support wakeup from D3_{cold} have an auxiliary power source (+3.3V_{aux}) to power the WAKE# logic which maintains connection of these WAKE# sources to the system board's WAKE# signal network even when the Link hierarchy's power (+3.3V) has been switched off.



This example assumes that all sources of WAKE# on the Add-in Card are powered by either the +3.3V or +3.3V_{aux} (V_{SOURCE}). If WAKE# from D3_{cold} is supported by some, but not all of the Add-in Card's functions that generate WAKE#, the Add-in Card designer must ensure that there is separate isolation control for each of the WAKE# generation power sources.

PCI Express component designers could choose to integrate the “power fail detect” isolation circuitry with their WAKE# output pin physically corresponding to the source of FET Q1. Alternatively, all isolation control logic could be implemented externally on the Add-in Card.

This example is meant as a conceptual aid and is not intended to prescribe an actual implementation.

2.4. SMBus (Optional)

The optional System Management Bus (SMBus) is a two-wire interface through which various system component chips can communicate with each other and with the rest of the system. It is based on the principles of operation of I²C.

SMBus provides a control bus for system and power management related tasks. A system may use SMBus to pass messages to and from devices instead of tripping individual control lines. Removing the individual control lines reduces pin count. Accepting messages ensures future expandability.

With SMBus, a device can provide manufacturer information, tell the system what its model/part number is, save its state for a suspend event, report different types of errors, accept control parameters, and return its status.

SMBus is described in *System Management Bus (SMBus) Specification*. Refer to this specification for DC characteristics and all AC timings. If the system board or Add-in Card supports SMBus, it must adhere to additional requirements that may be found in the *PCI Local Bus Specification*.

The system board provides pull-ups to the +3.3Vaux rail per the above specification and the components attached to these signals need to have a +3.3 V signaling tolerance.

2.4.1. Capacitive Load of High-power SMBus Lines

Capacitive load for each bus line includes all pin, wire, and connector capacitances. The maximum capacitive load affects the selection of the pull-up resistor or the current source to meet the rise time specifications of SMBus.

Normally, pin capacitance is defined as the total capacitive load of one SMBus device as seen in a typical manufacturer's data sheet. The value in the DC specifications (C_{OUT} in Table 2-6) is a recommended guideline so that two SMBus devices may, for example, be populated on an Add-in Card.

2.4.2. Minimum Current Sinking Requirements for SMBus Devices

While SMBus devices used in low-power segments have practically no minimum current sinking requirements due to the low pull-up current specified for low-power segments, devices in high-power segments are required to sink a minimum current of 4 mA while maintaining the $V_{OL2(max)}$ of 0.4 V. The requirement for 4 mA sink current determines the minimum value of the pull-up resistor that can be used in SMBus systems.

2.4.3. SMBus “Back Powering” Considerations

Unpowered devices connected to either a low-power or high-power SMBus segment must provide, either within the device or through the interface circuitry, protection against “back powering” the SMBus. Unpowered devices connected to high-power segments must meet leakage specifications in Chapter 3 of the *System Management Bus (SMBus) Specification*.

2.4.4. Power-on Reset

SMBus devices detect a power-on event in one of three ways:

- By detecting that power is being applied to the device
- By PERST# being asserted
- For self-powered or always-powered devices, by detecting that the SMBus is active (clock and data lines have gone high after being low for more than 2.5 s)

SMBus devices must respond to a power-on event by bringing the device into an operational state within t_{POR} , defined in Layer 1 of the *System Management Bus (SMBus) Specification*, after the device has been supplied power that is within the device's normal operating range. Self-powered or always-powered devices, such as Smart Batteries, are not required to do a complete power-on reset, but they must be in an operational state within 500 ms after the SMBus becomes active.

2.5. JTAG Pins (Optional)

The *IEEE Standard 1149.1, Test Access Port and Boundary Scan Architecture*, is included as an optional interface for PCI Express devices. *IEEE Standard 1149.1* specifies the rules and permissions for designing an 1149.1-compliant interface. Inclusion of a Test Access Port (TAP) on an Add-in Card allows boundary scan to be used for testing of the card on which it is installed. The TAP is comprised of four pins (optionally five) that are used to interface serially with a TAP controller within the PCI Express device.

TCK	in	<i>Test Clock</i> is used to clock state information and test data into and out of the device during operation of the TAP.
TDI	in	<i>Test Data Input</i> is used to serially shift test data and test instructions into the device during TAP operation.
TDO	out	<i>Test Output</i> is used to serially shift test data and test instructions out of the device during TAP operation.
TMS	in	<i>Test Mode Select</i> is used to control the state of the TAP controller in the device.
TRST#	in	<i>Test Reset</i> provides an asynchronous initialization of the TAP controller. This signal is optional in <i>IEEE Standard 1149.1</i> .

These TAP pins operate at +3.3 V, the same as the other single-ended I/O signals of the PCI Express connector. The drive strength of the TDO pin is not required to be the same as other PCI Express pins. The Add-in Card vendor must specify TDO drive strength. The direction of these TAP pins is defined from the perspective of the Add-in Card.

The system vendor is responsible for the design and operation of the 1149.1 serial chains (“rings”) required in the system. The signals are supplementary to the PCI Express interface. Additional information can be found in the *PCI Local Bus Specification*.

2.6. PWRBRK# Signal (Optional)

The PWRBRK# signal is an optional normative capability applicable to the CEM form factor. Only Add-in Cards that support Emergency Power Reduction connect to this pin. See Section 11.2.5 for AC termination requirements for this pin. Likewise, only systems that support the Emergency Power Reduction mechanism connect to this pin. The assertion and de-assertion of PWRBRK# are asynchronous to any system clock. An Add-in Card that supports Emergency Power Reduction must provide a weak pull-up on PWRBRK# (minimum 95 K Ω). A system that supports Emergency Power Reduction must provide a stronger pull-up on PWRBRK#. These pull-up resistor values must ensure meeting the rise time specification of $T_{PWRBRK\#}$.

The PWRBRK# signal is used to communicate requests to enter and exit the Emergency Power Reduction State. Refer to the *PCI Express Base Specification*.

PWRBRK# is an open-drain, active low signal that is driven low by an external enclosure component. When asserted, Add-in Cards that support Emergency Power Reduction must quickly reduce their power consumption. When de-asserted, Add-in Cards that support Emergency Power Reduction are permitted to resume normal power consumption. The Add-in Card must debounce this input to avoid thrashing the system with rapid transitions in and out of the Emergency Power Reduction State.

This mechanism is an emergency fail-safe intended to be used to prevent system damage and is not intended to provide normal dynamic power management. The external enclosure must control how it asserts/de-asserts this signal to avoid thrashing the system with rapid transitions in and out of the Emergency Power Reduction State. The amount of power consumed in the Emergency Power Reduction state is communicated through the Power Budgeting extended capability as defined in the *PCI Express Base Specification*. The time allowed to achieve this power reduction ($T_{PWRBRK\#-AIC-ENTER-LP-MODE}$) is defined in Table 2-7.

Add-in Cards that support Emergency Power Reduction may contain any mix of Devices that advertise support for PWRBRK# or that don't advertise such support. Software is not required to configure or enable use of PWRBRK#. Software can optionally use the mechanisms defined in the *PCI Express Base Specification* to determine support for PWRBRK# and, if supported, to determine the associated power saving. Software can detect that a supporting Function has entered the Emergency Power Reduction State.

Electrical specifications for PWRBRK# at the PCI Express connector are defined in Table 2-6 and Figure 2-9. Timing requirements are defined in Table 2-7 and Figure 2-10.

PWRBRK# signal may be bused to multiple PCI Express Add-in Card connectors, forming a single output connection at the external enclosure component, or individual connectors may have individual connections to the external enclosure component.

2.7. MFG Signal (Optional)

The MFG signal is an optional signal applicable only to Add-in Cards (AIC) that support a manufacturer-specific test mode, and as such all functional requirements are outside the scope of this specification. On System Boards, the MFG pin is not connected.

Electrical specifications of the MFG signal are defined in Table 2-6.

The MFG pin must be AC terminated as specified in Section 11.2.5, and must not have any impact to normal AIC operation.

2.8. CLKREQ# Signal (Optional)

The CLKREQ# signal is an open drain, active low signal that is driven low by the add-in card to request that the PCI Express reference clock be available (active clock state) to allow the PCI Express interface to send/receive data. Operation of the CLKREQ# signal is determined by the state of the Enable Clock Power Management bit in the Link Control register. When disabled, the CLKREQ# signal shall be asserted at all times whenever power is applied to the card, with the exception that it may be de-asserted during L1 PM Substates. When enabled, the CLKREQ# signal may be de-asserted during an L1 Link state.

The CLKREQ# signal is also used by the L1 PM Substates mechanism. In this case, CLKREQ# can be asserted by either the system or add-in card to initiate an L1 exit. See the PCI Express Base Specification for details on the functional requirements for the CLKREQ# signal when implementing L1 PM Substates.

Whenever dynamic clock management is enabled and when a card stops driving CLKREQ# low, it indicates that the device is ready for the reference clock to transition from the active clock state to a parked (not available) clock state. Reference clocks are not guaranteed to be parked by the host system when CLKREQ# gets de-asserted and module designs shall be tolerant of an active reference clock even when CLKREQ# is de-asserted by the module.

The card must drive this signal low during power up, whenever it is reset, and whenever it requires the reference clock to be in the active clock state. Whenever PERST# is asserted, including when the device is not in D0, CLKREQ# shall be asserted.

It is important to note that the PCI Express device must delay de-assertion of its CLKREQ# signal until it is ready for its reference clock to be parked. Also, the device must be able to assert its clock request signal, whether the reference clock is active or parked, when it needs to put its Link back into the L0 Link state. Finally, the device must be able to sense an electrical idle break on its up-stream-directed receive port and assert its clock request, whether the reference clock is active or parked.

The assertion and de-assertion of CLKREQ# are asynchronous with respect to the reference clock.

Add-in Cards that do not implement a PCI Express interface shall leave this output unconnected on the card.

CLKREQ# has additional electrical requirements over and above standard open drain signals that allow it to be shared between devices that are powered off and other devices that may be powered on. The additional requirements include careful circuit design to ensure that a voltage applied to the CLKREQ# signal network never causes damage to a component even if that component's power is not applied.

Additionally, the device must ensure that it does not pull CLKREQ# low unless CLKREQ# is being intentionally asserted in all cases, including when the related function is in D3_{cold}. This means that any component implementing CLKREQ# must be designed such that:

- Unpowered CLKREQ# output circuits are not damaged if a voltage is applied to them from other powered “wire-ORed” sources of CLKREQ#.
- When power is removed from its CLKREQ# generation logic, the unpowered output does not present a low impedance path to ground or any other voltage.

These additional requirements ensure that the CLKREQ# signal network continues to function properly when a mixture of powered and unpowered components have their CLKREQ# outputs wire-ORed together. It is important to note that most commonly available open drain and tri-state buffer circuit designs used “as is” do not satisfy the additional circuit design requirements for CLKREQ#.

2.8.1. Power-up Requirements

CLKREQ# is asserted in response to PERST# assertion. On power up, CLKREQ# must be asserted by a PCI Express device within a delay (TPVCRL) from the power rails achieving specified operating limits and PERST# assertion. This delay is to allow adequate time for the power to stabilize on the card and certain system functions to start prior to the card starting up. CLKREQ# may not be de-asserted while PERST# is asserted.

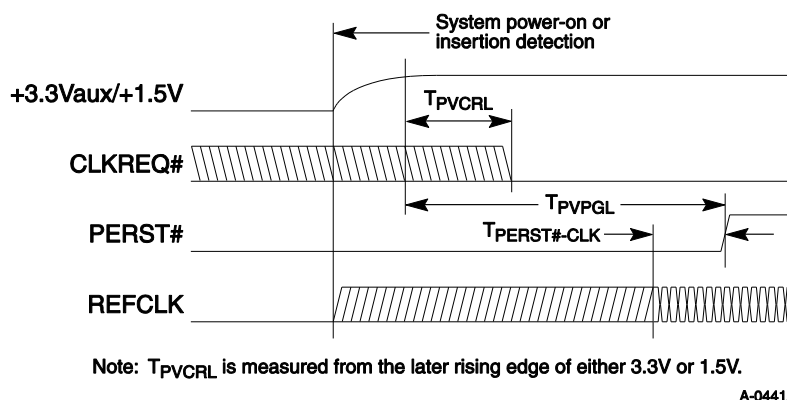


Figure 2-7. Power-Up CLKREQ# Timing

Table 2-4. Power-Up CLKREQ# Timing

Symbol	Parameter	Min	Max	Unit
TPVCRL	Power Valid to CLKREQ# Output active		100	μs
TPVPGL	Power Valid to PERST# Input inactive	1		ms
TPERST#-CLK	REFCLK stable before PERST# inactive	100		μs

The system is required to have the reference clock for a PCI Express device in the parked clock state prior to device power-up. The state of the reference clock is undefined during device power-up, but it must be in the active clock state for a setup time TPERST#-CLK prior to PERST# de-assertion.

2.8.2. Dynamic Clock Control

After a PCI Express device has powered up and whenever its upstream link enters the L1 link state, it shall allow its reference clock to be turned off (put into the parked clock state). To accomplish this, the device de-asserts CLKREQ# (high) and it must allow that the reference clock will transition to the parked clock state within a delay (TCRHoff).

To exit L1, the device must assert CLKREQ# (low) to re-enable the reference clock. After the device asserts CLKREQ# (low) it must allow that the reference clock will continue to be in the parked clock state for a delay (TCRLon) before transitioning to the active clock state. The time that it takes for the device to assert CLKREQ# and for the system to return the reference clock to the active clock state are serialized with respect to the remainder of L1 recovery. This time must be considered when the device is reporting its L1 exit latency.

When the PCI Express device supports and is enabled for Latency Tolerance Reporting (LTR), the device must allow that the reference clock transition to the active clock state may be additionally delayed by the system up to a maximum value consistent with requirements for the LTR mechanism. During this delay, the reference clock must remain parked. When exiting the parked state following the delay, the clock must be stable and valid within 400 ns.

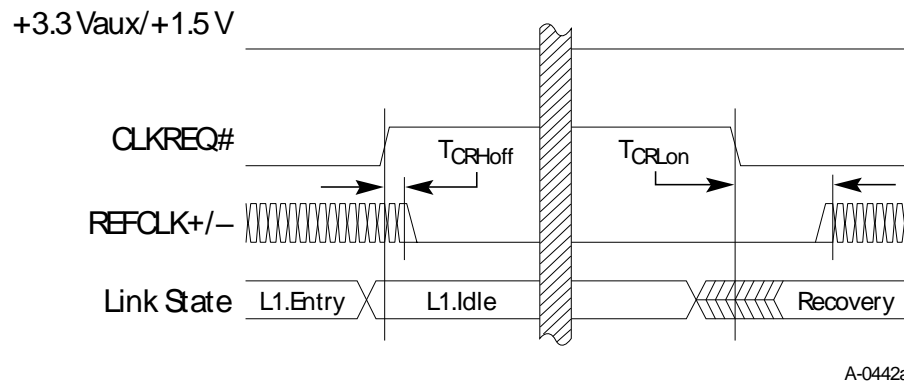


Figure 2-8. CLKREQ# Clock Control Timings

All links attached to a PCI Express device must complete a transition to the L1.Idle state before the device can de-assert CLKREQ#. The device must assert CLKREQ# when it detects an electrical idle break on any receiver port. The device must assert CLKREQ# at the same time it breaks electrical idle on any of its transmitter ports to minimize L1 exit latency.

Table 2-5. CLKREQ# Clock Control Timings

Symbol	Parameter	Min	Max	Unit
T_{CRHoff}	CLKREQ# de-asserted high to clock parked	0		ns
T_{CRLon}	CLKREQ# asserted low to clock active		400	ns

T_{CRLon} is allowed to exceed this value when LTR is supported and enabled for the device.

There is no maximum specification for T_{CRHoff} and no minimum specification for T_{CRLon} . This means that the system is not required to implement reference clock parking or that the implementation may not always act on a device de-asserting CLKREQ#.

A device should also de-assert CLKREQ# when its link is in L2 or L3, much as it does during L1.

2.9. Auxiliary Signal Parameter Specifications

2.9.1. DC Specifications

Table 2-6 lists the auxiliary signal DC specifications for PERST#, WAKE#, CLKREQ#, SMBus, PWRBRK#, and MFG.

Table 2-6: Auxiliary Signal DC Specifications – PERST#, WAKE#, CLKREQ#, SMBus, MFG, and PWRBRK#

Symbol	Parameter	Conditions	Min	Max	Unit	Notes
V _{IL1}	Input Low Voltage		-0.5	+0.8	V	2, 6, 7
V _{IH1}	Input High Voltage		+2.0	V _{CC3_3} + 0.5	V	2, 6, 7
V _{IL2}	Input Low Voltage		-0.5	+0.8	V	4
V _{IH2}	Input High Voltage		+2.1	+3.3 V _{aux} + 0.5	V	4
V _{OL1}	Output Low Voltage	4.0 mA		+0.2	V	1, 3
V _{HMAX}	Max High Voltage			V _{CC3_3} + 0.5	V	3
V _{OL2}	Output Low Voltage	4.0 mA		+0.4	V	1, 4
I _{in_lkg}	Input Leakage Current	0 to +3.3 V	-10	+10	μA	2, 4, 7
I _{out_lkg}	Output Leakage Current	0 to +3.3 V	-50	+50	μA	3, 5
C _{in}	Input Pin Capacitance			20	pF	2, 7, 9
C _{out}	Output (I/O) Pin Capacitance			30	pF	3, 4, 9
R _{PULL-UP}	Pull-up Resistance		9	60	kΩ	8

Notes:

1. Open-drain output a pull-up is required on the system board. There is no V_{OH} specification for these signals. The number given is the maximum voltage that can be applied to this pin.
2. Applies to PERST#.
3. Applies to WAKE# and CLKREQ#.
4. Applies to SMBus signals SMBDAT and SMBCLK.
5. Leakage at the pin when the output is not active (high impedance).
6. Applies to WAKE# driven by upstream components for signaling of OBFF indications as received at the input of downstream components.
7. Applies to PWRBRK#.
8. Applies to CLKREQ# pull-up on host system.
9. As measured at the Add-in Card edge-finger.

2.9.2. AC Specifications

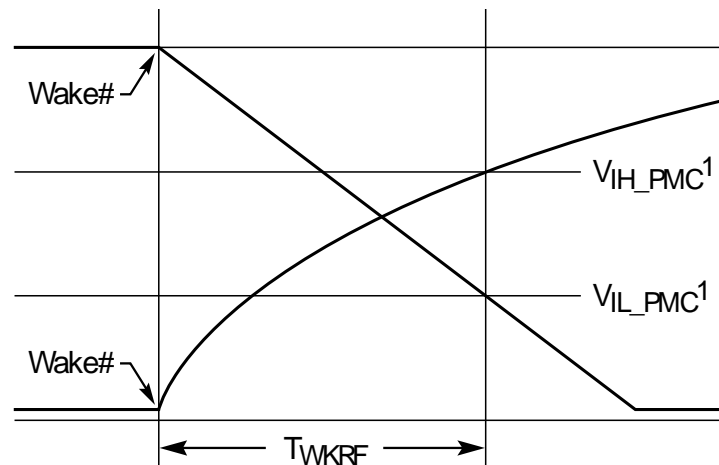
Table 2-7 lists the power sequencing and Reset signal timing.

Table 2-7: Power Sequencing and Reset Signal Timings

Symbol	Parameter	Min	Max	Units	Notes	Figure
T _{PVPERL}	Power stable to PERST# inactive	100		ms	1	Figure 2-3
T _{PERST-CLK}	REFCLK stable before PERST# inactive	100		μs	2	Figure 2-3
T _{PERST}	PERST# active time	100		μs		Figure 2-4
T _{FAIL}	Power level invalid to PERST# active		500	ns	3	Figure 2-6
T _{PERSTSLEW}	Slew rate of PERST# transition to inactive	50		mV/ns	7	
T _{WKRF}	WAKE# rise – fall time		100	ns	4	Figure 2-9
T _{WAKE-TX-MIN-PULSE}	Minimum WAKE# pulse width; applies to both active-inactive-active and inactive-active-inactive cases	300		ns	5	
T _{WAKE-FALL-FALL-CPU-ACTIVE}	Time between two falling WAKE# edges when signaling CPU Active	700	1000	ns	5	
T _{PWRBRKRF}	PWRBRK# rise – fall time		100	ns	6	Figure 2-10
T _{PWRBRK-FALL-RISE-ACTIVE}	Time PWRBRK# is active	1		ms	6	Figure 2-10
T _{PWRBRK-RISE-FALL-INACTIVE}	Time PWRBRK# is inactive	1		ms	6	Figure 2-10
T _{PWRBRK-AIC-ENTER-LP-MODE}	Time for Add-in Card to enter low power mode		10	μs		Figure 2-10

Notes:

- Any supplied power is stable when it meets the requirements specified for that power supply.
- A supplied reference clock is stable when it meets the requirements specified for the reference clock. The PERST# signal is asserted and de-asserted asynchronously with respect to the supplied reference clock.
- The PERST# signal must be asserted within T_{FAIL} of any supplied power going out of specification.
- Measured from WAKE# assertion/de-assertion to valid input level at the system PM controller. Since WAKE# is an open-drain signal, the rise time is dependent on the total capacitance on the platform and the system board pull-up resistor. It is the responsibility of the system designer to meet the rise time specification.
- Only for OBFF using WAKE# signaling: Refer to timing requirement for indicating an active window.
- Refers to PWRBRK# timing diagram in Figure 2-10.
- The slew rate of PERST# transition to inactive through its logic input switching range (V_{IL1} max to V_{IH1} min, see Table 2-6)



Note 1: Power Management Controller input switching levels are platform dependent and are not set by this specification.

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Figure 2-9: WAKE# Rise and Fall Time Measurement Points

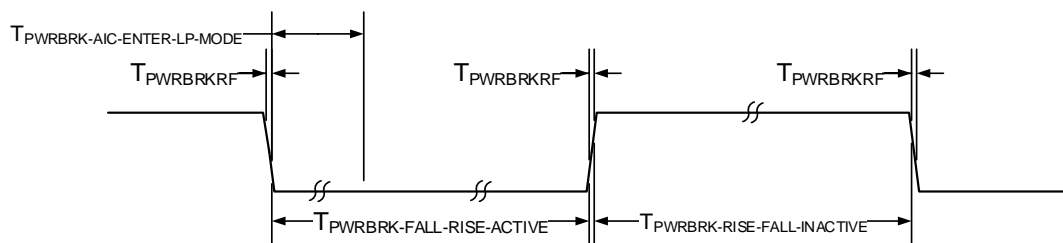


Figure 2-10: PWRBRK# Timing Requirement Diagram

3. Hot Insertion and Hot Removal

In this chapter, all references to hot insertion and hot removal apply to the PCI Express CEM form factor. CEM support of hot insertion and hot removal is confined to Add-in Cards that do not require supplemental power through the auxiliary power connectors. Other PCI Express form factors implement hot insertion and hot removal differently.

3.1. Scope

This specification natively supports hot insertion/hot removal of PCI Express Add-in Cards that do not use an auxiliary power connector. However, hardware support of hot insertion/hot removal on the system board is optional. Since the PCI Express evolutionary form factor is designed as a direct PCI connector replacement and utilizes an edge card connector, the PCI Express Native Hot Plug model is based on the standard usage model defined in the *PCI Standard Hot Plug Controller and Subsystem Specification*.

Section 3.2 describes the Add-in Card presence detect and PCI Express Native Hot Plug signals. For a detailed explanation of the register requirements and standard usage model, see the *PCI Express Base Specification*.



Note: CEM 5.0 supports managed Hot Plug only. Surprise Hot Plug is no longer supported in CEM 5.0.

3.2. Presence Detect

If implemented, the PCI Express Hot Plug controller on the system board detects the presence of an Add-in Card using the PRSNT2# signal as shown in Figure 3-1. It is the responsibility of the Downstream Port connected to the slot to determine the presence of the Add-in Card and set the presence detect bit in the appropriate register as described in the *PCI Express Base Specification*. In addition to the Hot Plug controller, the system board may use the PRSNT2# signal to recognize the presence of the Add-in Card to enable other auxiliary signals. The two signals, PRSNT1# and PRSNT2#, described in Figure 3-1, are required on the PCI Express connector and must be supported by all PCI Express Add-in Cards.



Note: Figure 3-1 reflects the legacy Last Mate/First Break PRSNT# Add-in Card edge-finger scheme, to support surprise Hot Plug. This has been deprecated for CEM 5.0 Add-in Cards, but may be supported at the vendor's discretion for CEM 5.0 system boards.

Both PRSNT1# and PRSNT2# signals are required to detect the presence of the Add-in Card. The PRSNT1# and PRSNT2# Add-in Card edge-fingers must be implemented to enable the auxiliary signals. All Add-in Card edge-fingers, including PRSNT1# and PRSNT2#, must be the same length, 3.0 mm.



IMPLEMENTATION NOTE

This requirement is a change from earlier versions of this specification, which required a shorter edge-finger for PRSNT1# and PRSNT2#.

Unused PRSNT2# card edge-fingers on x4, x8, and x16 Add-in Cards must be present. CEM 5.0 compliant system boards may implement support for Hot Plug to remain compatible with legacy add-in cards. The mechanical details are provided in Chapter 6.

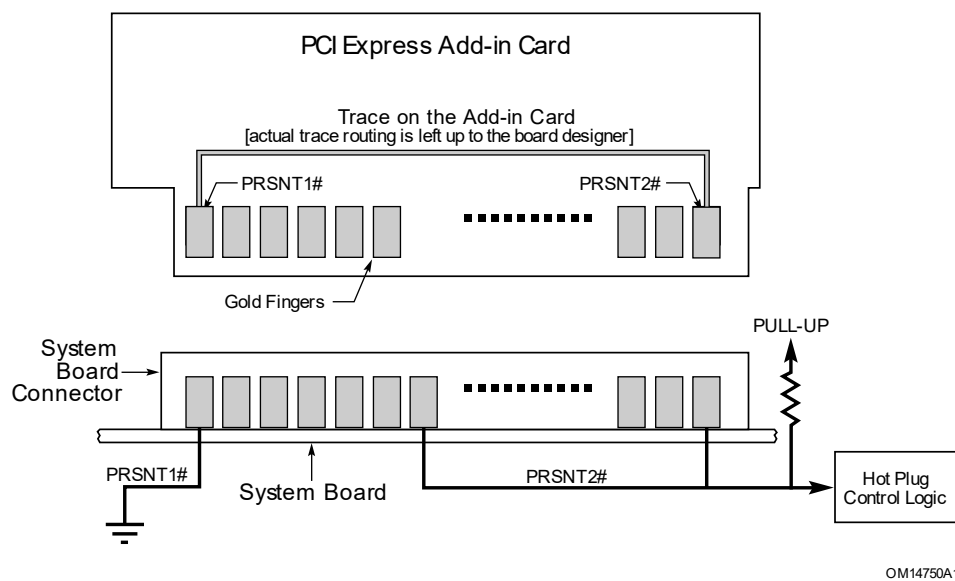


Figure 3-1: Presence Detect in a Hot Plug Environment

It is required that all PCI Express Add-in Cards implement full length card edge-fingers. There are more than one PRSNT2# pin defined in the x4, x8, and x16 PCI Express connectors; these are needed to support up-plugging. The PRSNT1# signal is connected to the most distant PRSNT2# signal position on all Add-in Cards with a single trace in between them as shown in Figure 3-1. For example, a x4 Add-in Card would connect PRSNT1# with PRSNT2# on pin B31, a x8 Add-in Card would connect PRSNT1# with PRSNT2# on pin B48, and a x16 Add-in Card would connect PRSNT1# with PRSNT2# on pin B81. See Table 6-1 for connector pin numbering and definition. If the system board designer chooses to implement presence detect support, the system board must connect PRSNT1# to ground and separately connect all the PRSNT2# pins together to a single pull-up resistor, as shown in Figure 3-1. The system board designer determines the pull-up resistor voltage and associated use of applicable Hot Plug control logic. If the system board designer chooses not to implement presence detect support, PRSNT1# and PRSNT2# connector pins on the system board must be left unconnected, grounded, or terminated with the AC terminated scheme described in Section 11.2.5. All PRSNT2# pin positions within the connector width on the Add-in Card must be populated, and connected with an AC-terminated edge-finger, as described in Sections 11.2.4 and 11.2.5.



Note: Support for down-plugging is outside the scope of this specification. However, systems that support down-plugging should be aware that the presence detect method described in this section will not work with down-plugged Add-in Cards.



IMPLEMENTATION NOTE

Connectors with Underpopulated Lanes

Even though a connector may not populate all the possible lanes, the system board that implements Hot Plug support must always connect all the PRNST2# pins that are possible based on the physical connector size, regardless of the number of lanes populated. As an example, a x8 Add-in Card may plug into a x8 connector with a x4 Link only, the system board shall have the three PRSNT2# pins (B17, B31 and B48) connected. This is required to sense the presence of the x8 Add-in Card in a x8 connector that supports a x4 Link only. See Section 11.5 for card interoperability discussions.

4. Electrical Requirements

Power delivery requirements defined in this chapter apply not only to the Add-in Cards, but also to connectors, cables, and systems.

4.1. Power Supply Requirements

Systems that mount PCI Express CEM Connectors are required to provide both the +12V and +3.3V rails to every PCI Express CEM Connector in the system. A third optional +3.3Vaux rail can also be provided.

The +3.3Vaux rail must be supplied to the PCI Express CEM Connector if the system supports wakeup or the system supports SMBus operation while in D3_{cold}, otherwise it may be supplied at the system board designers' discretion. However, if +3.3Vaux is supplied to the PCI Express CEM Connector, the +3.3Vaux rail must be supplied to all PCI Express CEM Connectors in the system. A third optional +3.3Vaux rail can also be provided.

Table 4-1 provides the required specifications for the power supply rails available at the PCI Express CEM Connectors. Table 4-2 provides the required specifications for any Auxiliary Power connectors (and cables) to the PCI Express CEM Add-in Card. These Auxiliary Power connectors (and cables) should not be confused with the +3.3Vaux rail power from the PCI Express CEM Connector.

The System designer is responsible for ensuring the power delivered to the PCI Express CEM Connector, and any Auxiliary Power Connectors, meets the specifications called out in Table 4-1 and Table 4-2 as its minimum limit requirements. The Card designer is responsible for ensuring the power consumed at the PCI Express CEM Add-in Card edge-finger, and any Auxiliary Power Connectors falls within the limits called out in Table 4-1 and Table 4-2.

Table 4-1: Power Supply Rail Requirements- PCI Express CEM Connector / Edge-Finger

Power Rail	10 W Slot	25 W Slot	75 W Slot
+3.3 V (V_{cc3_3})			
Voltage tolerance	$\pm 9\%$	$\pm 9\%$	$\pm 9\%$
Supply Current	3.0 A (max)	3.0 A (max)	3.0 A (max)
Capacitive Load	1000 μ F (max)	1000 μ F (max)	1000 μ F (max)
+12 V			
Voltage tolerance	$\pm 8\%$	$\pm 8\%$	$\pm 8\%$
Supply Current	0.5 A (max)	2.1 A (max)	5.5 A (max)
Capacitive Load	300 μ F (max)	1000 μ F (max)	2000 μ F (max)
+3.3 Vaux			
Voltage tolerance	$\pm 9\%$	$\pm 9\%$	$\pm 9\%$
Supply Current			
Wakeup Enabled or Aux Power PM Enabled,	375 mA (max)	375 mA (max)	375 mA (max)
Wakeup Disabled or Aux Power PM Disabled	20 mA (max)	20 mA (max)	20 mA (max)
Capacitive Load	150 μ F (max)	150 μ F (max)	150 μ F (max)

Notes:

1. The maximum current slew rate for each Add-in Card shall be no more than 0.1 A/ μ s.
2. Each Add-in Card shall limit its bulk capacitance on each power rail to less than the values shown in this table.

Table 4-2: Power Supply Rail Requirements - Auxiliary Power Connectors

Power Rail	2x3 Connector	2x4 Connector	12VHPWR Connector	48VHPWR Connector
+12V				
Voltage Tolerance	+5%/-8%	+5%/-8%	+5%/-8%	N/A
Supply Current	6.25 A (max)	12.5 A (max)	55 A (max)	
+48V				
Voltage Tolerance	N/A	N/A	N/A	40.0 to 59.5 V
Supply Current				15 A (max)

Within each Auxiliary Power connector, the power supplied to all power pins must belong to the same power supply rail. For all Add-in Card Auxiliary Power requirements, see Chapter 5.

PCI Express Add-in Cards must accommodate the maximum voltage variation between the +12V from the PCI Express edge connector slot and any Auxiliary connector +12V inputs.

4.2. Power Consumption

This specification supports multiple PCI Express CEM Add-in Card edge-finger mechanical widths based on number of lanes for system implementation. For each size of PCI Express CEM Add-in Card edge-finger mechanical width, the maximum initial power consumption from the edge connector must be limited at system power up until software configures it for a different power (refer to the *PCI Express Base Specification* for information on the power configuration mechanisms).

The following tables provide the maximum power consumption for each PCI Express CEM Add-in Card edge-finger mechanical width and form factor:

- As permitted at System Power Up (Table 4-3)
- As permitted after Software Configuration (Table 4-4)

**Table 4-3: PCI Express CEM Add-in Card Edge-Finger
Initial Permitted Power Draw at System Power Up**

Card Connector Interface	Power Draw Permitted at System Power Up
x1	10 W available from edge connector
x4/x8/x16	25 W available from edge connector

**Table 4-4: PCI Express CEM Add-in Card Edge-Finger
Maximum Permitted Power Draw after Software Configuration**

Card Connector Interface	Maximum Power Draw Permitted after Software Configuration
x1 low-profile	10 W available from edge connector
x1 half-length	10 W available from edge connector
x1 full-length—standard height	75 W available from edge connector
x4 / x8 / x16	75 W available from edge connector

Following are additional power considerations:

- The card power limits represent the associated system board power requirements for the slot.
- Power for Add-in Cards that support a 75 W maximum power consumption can be drawn via a combination of +12V, +3.3V and +3.3Vaux rails.
 - Each rail's maximum draw is limited as defined in Table 4-1
 - The combined draw across all power rails on the Add-in Card edge-finger must not exceed 75 W.
 - > The power limits assume that enough cooling is provided to the slot by the chassis environment.

The PCI Express Card Electromechanical Specification supports card power up to 600 W.

- For power levels above 75 W, the PCI Express edge connector power must be supplemented by the use of Auxiliary Power Connector(s) as described below in Chapter 5.

4.3. Power Budgeting Capability

The Power Budgeting Capability structure, as defined in the *PCI Express Base Specification*, is implemented for:

- Cards capable of using more power than initially allowed at power-up (see Section 4.2).
- Cards utilizing auxiliary power connections (e.g. 150 W, 225 W, 300 W, 600 W, etc.).
- Sustained Thermal and Maximum Thermal values include all thermal power that is produced by the card.
- Populated values shall include all power used by the card including power drawn from auxiliary power connections.
- For multi-device cards, an instance of the Power Budget Capability structure reports power at a device or card level. For multi-device cards, such as a Switch with devices behind it, system software aggregates all instances of the Power Budgeting Capability structure implemented at or beneath the base device of the card.

4.4. Power Supply Sequencing

There is no specific requirement for power supply sequencing of the power supply rails, whether delivered by the system board or cables. They may come up or go down in any order. The system must assert the PERST# signal whenever any of the power rails goes outside of the specified tolerances (see Section 2.2 for specific information on the function and proper use of the PERST# signal).

If a PCI Express Add-in Card requires power supply rail sequencing, it is the responsibility of the Add-in Card designer to provide appropriate circuitry on the Add-in Card to meet any power supply rail sequencing requirements.

4.5. Power Supply Decoupling

Due to the low level signaling of the PCI Express interface, it is strongly recommended that sufficient decoupling of all power supplies be provided. This is recommended to ensure that power supply noise does not interfere with the recovery of data from a remote PCI Express device. Some basic guidelines to help ensure a quiet power supply are provided below.

The following points are guidelines only. It is the responsibility of the Add-in Card designer to properly test the design to ensure that Add-in Card circuitry does not create excessive noise on power supply or ground signals at the Add-in Card edge-fingers.

- The Add-in Card device decoupling capacitance must average 0.01 μF per device power rail pin (for all devices on the Add-in Card).
- The trace length between a decoupling capacitor and the power supply or ground via must be less than 5.08 mm (0.2 inches) and be a minimum of 0.508 mm (0.02 inches) in width.
- A bulk decoupling capacitor (greater than 10 μF) is recommended at the Add-in Card edge-finger for each power supply.
- A bulk decoupling capacitor (greater than 10 μF) is recommended on each power supply used within a device on the Add-in Card. This bulk decoupling capacitor must be near the Add-in Card device.

4.6. Electrical Topologies and Link Definitions

The remainder of this chapter describes the electrical characteristics of PCI Express Add-in Cards. The electrical characteristic at the card interface is defined in terms of electrical budgets. This budget allocation decouples the electrical specification for the system designer and the card vendor and ensures successful communication between the PCI Express signal input and output Links at the system board and Add-in Card interface. Unless otherwise indicated, the specifications contained herein apply to all high-speed signals of each interface width definition. The signaling rate for encoded data is 32.0 GT/s, 16.0 GT/s, 8.0 GT/s, 5.0 GT/s, or 2.5 GT/s and the signaling is point-to-point. Requirements are called out separately for 32.0 GT/s, 16.0 GT/s, 8.0 GT/s, 5.0 GT/s, and 2.5 GT/s signaling rates. System Boards and Add-in Cards must support at least 2.5 GT/s signaling and must support all data rates below the maximum data rate the system board or Add-in Card supports.

4.6.1. Topologies

The electrical topologies supported by this specification are:

- PCI Express devices across one connector on a system with a system board and an Add-in Card.
- PCI Express devices across two connectors on a system with a system board, a riser card, and an Add-in Card.

A riser card is permitted to contain a Switch or a Retimer, between the two connectors on the system.



IMPLEMENTATION NOTE

Two connector topologies with higher loss are likely to need Retimers, especially if they support the 32.0 GT/s or 16.0 GT/s data rates. Two connector topologies with higher loss are likely to need Retimers, especially if they support the 32.0 GT/s or 16.0 GT/s data rates.

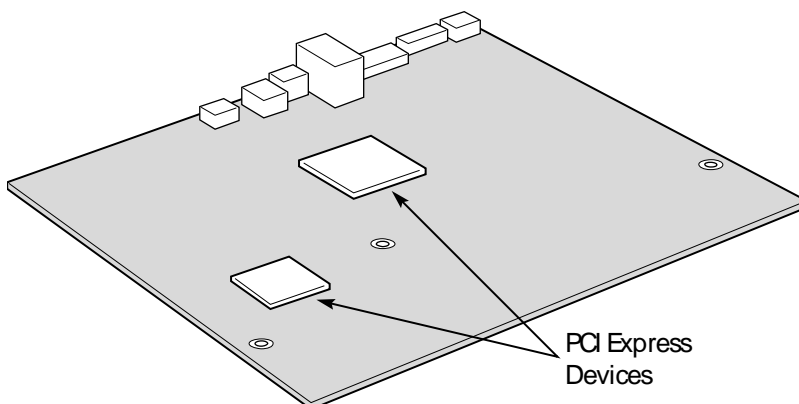
The number of Retimers on a PCI Express link (between an up-stream port and a down-stream port) is limited to two due to protocol limitations.

The maximum number of Retimers on a System board interconnect (including Riser) is two.

The maximum number of Retimers on an Add-in Card and any other interconnect beyond the PCI Express Connector is limited to one.

The PCI-SIG protocol does not support more than two Retimers in a link (between each upstream and downstream port). If there are more than two Retimers present, link training may fail. It is expected in most scenarios that there will be zero or one Retimers before the Add-in Card PCI Express connector on the system board and zero Retimers on the Add-in Card. The system integrator must exercise caution in selecting components since it is physically possible to combine a System Board with two Retimers and an Add-in Card component with one Retimer causing interoperability problems resulting from having a total of three Retimers in a link.

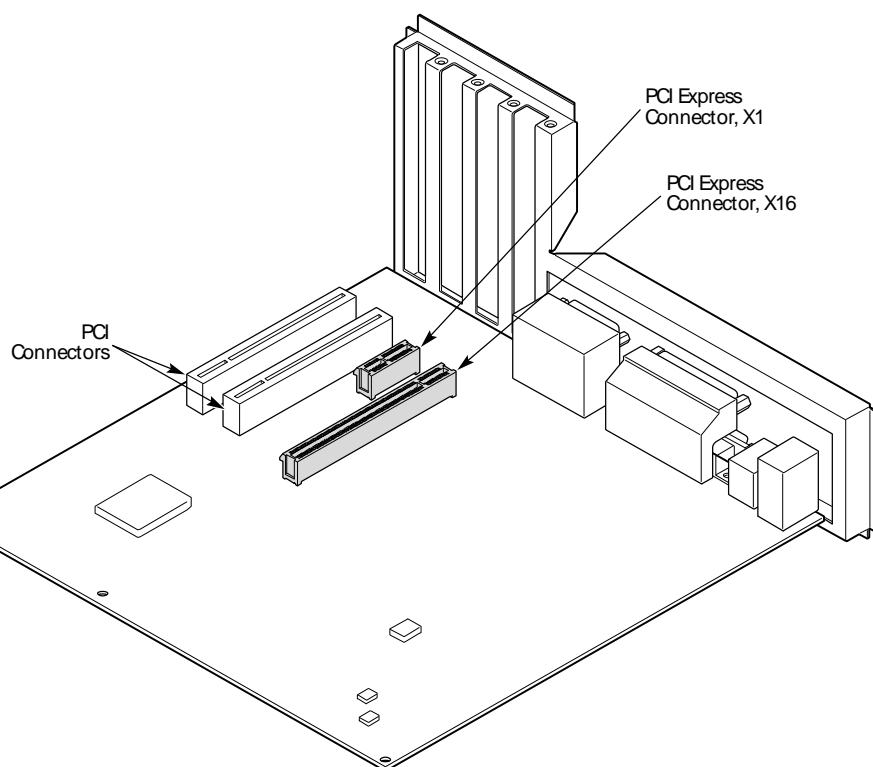
This specification supports only the one and two connector topologies. The “PCI Express on-board” configuration is used for two-PCI Express devices on a common PCB (see Figure 4-1) and lies outside the scope of this document. Since there are no Add-in Cards involved in this topology, refer to the *PCI Express Base Specification*, for implementation of this topology.



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Figure 4-1: PCI Express on the System Board

The topology of PCI Express with one connector allows a plug-in PCI Express Add-in Card to interface with a system board using a PCI Express vertical edge connector (Figure 4-2). In this topology, only one connector-card interface exists:



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Figure 4-2: PCI Express Connector on System Board with an Add-in Card

The topology of “PCI Express with two connectors on a riser card” allows for a plug-in PCI Express Add-in Card to interface with a riser card using a PCI Express connector (Figure 4-3). The riser card plugs to the system board using another riser connector (either PCI Express or another connector). In this topology, two connector-card interfaces exist. The riser card is part of the system electrical specifications and must be included during System compliance testing.

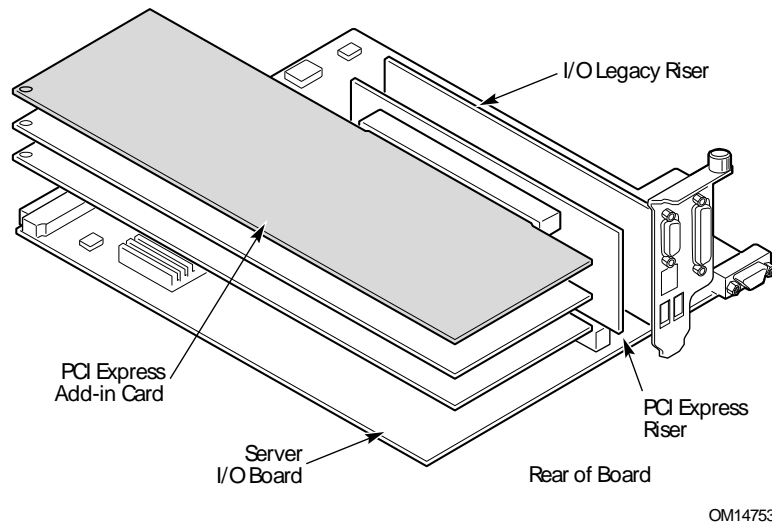


Figure 4-3: PCI Express Connector on a Riser Card with an Add-in Card

4.6.2. Link Definition

Typical PCI Express Links consist of the following:

- Transmitters/Receivers on an ASIC on a system board
- Package fan-in-out trace topologies
- PCB coupled microstrip and/or stripline
- Vias for layer transitions
- Optional proprietary PCI Express connector and riser card interface
- Optional riser card with microstrip and/or stripline trace
- PCI Express connector and Add-in Card interface
- Coupled microstrip line and/or stripline traces on Add-in Card
- AC-coupling capacitors
- Transmitter/Receivers on an ASIC on the Add-in Card

The electrical parameters for the Link are subdivided into two components (Figure 4-4):

- Add-in Card
- System board and PCI Express connector (and riser card with associated connector if it exists)

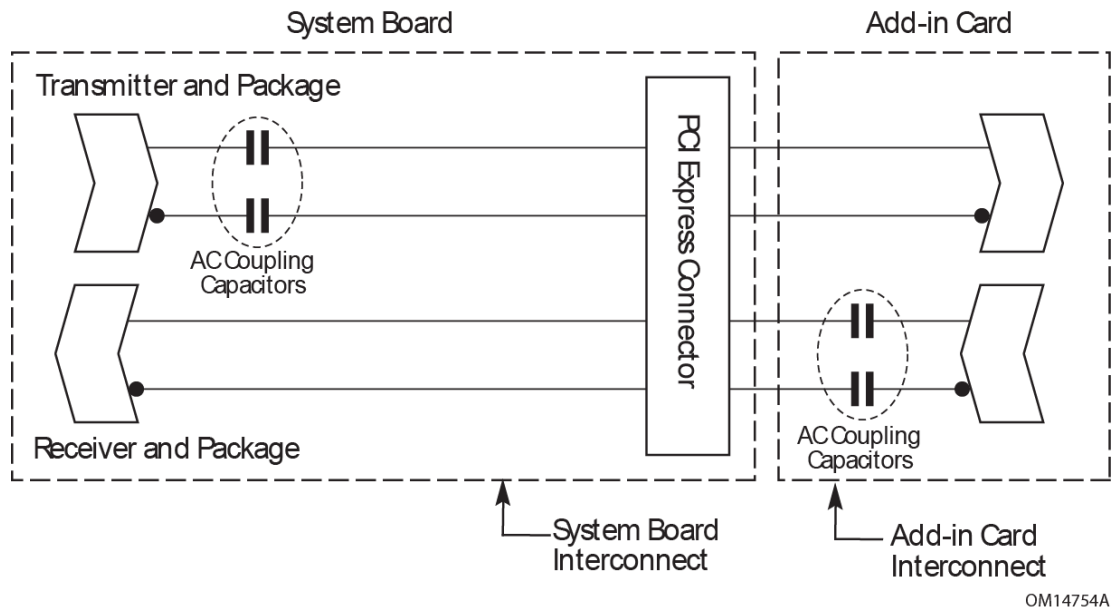


Figure 4-4: Link Definition for Two Components

The electrical impact on the Link due to discontinuities such as vias, bends, and test-points must be included in the respective components.

4.7. Electrical Budgets

A budget is defined for each of the following electrical parameters associated with the Link:

- AC coupling capacitors
- Insertion Loss
- Jitter
- Lane-to-Lane skew
- Crosstalk
- Transmitter De-emphasis and Equalization Skew within a differential pair
- Differential data trace impedance
- Differential data trace propagation delay

The electrical budgets are different for each of the two Link components:

- Add-in Card budget
- System board and PCI Express connector budgets

The interconnect Link budget allocations associated with the Transmitters and Receivers differ. This is to account for any electrical characteristics the AC coupling capacitors may contribute to the Link.

4.7.1. AC Coupling Capacitors

The PCI Express Add-in Card and system board shall incorporate AC coupling capacitors on the Transmitter differential pair. This is to ensure blocking of the DC path between the PCI Express Add-in Card and the system board. The specific capacitance values are specified in the *PCI Express Base Specification*.

Attenuation or jitter caused by the coupling capacitors must be accounted for as part of the budget allocation for the physical interconnect component's path on which the capacitors are mounted. There may be parasitic effects associated with the component's placement as mounted on the printed circuit board.

4.7.2. Insertion Loss Values (Voltage Transfer Function)

Appendix A contains background information on maximum insertion loss assumptions that were made in computing the 2.5 GT/s eye diagram requirements. This section is provided only for information purposes.

4.7.3. Jitter Values

The maximum jitter values in terms of percentage of Unit Interval (UI) are specified for the system board and the Add-in Card. Refer to the *PCI Express Base Specification* for UI values for each data rate. The jitter associated with the riser card and associated proprietary connector will be part of the system board jitter budget. The jitter values are defined with respect to 100 Ω differential termination, realized as two 50 Ω resistances. These resistances are referenced to ground at the interface (see Figure A-1).

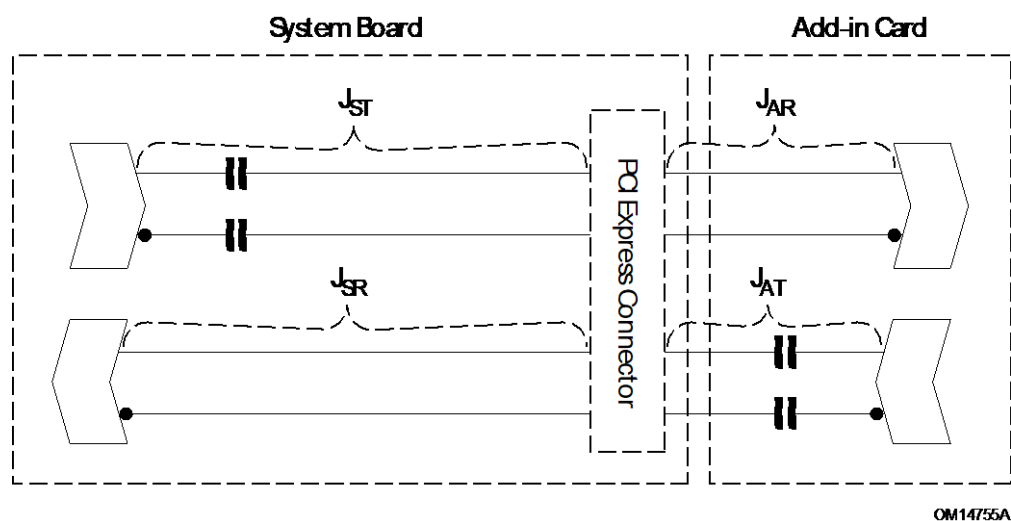


Figure 4-5: Jitter Budget

The total system jitter budget is derived with the assumption of a minimum R_j for each of the four budget items. This minimum R_j component is used to determine the overall system budget. The probability distribution of the R_j component is at the Bit Error Rate (BER) indicated and is Gaussian. See Table 4-5 for total system jitter budget for 2.5 GTs signals.

For any jitter distribution, the total T_j must always be met at the BER. The R_j of the components are independent and convolve as the root sum square (see Table 4-6). Tradeoffs of R_j and D_j are allowed, provided the total T_j is always met. More information on the calculation of the system budget can be found in *PCI Express Jitter and BER*.

Table 4-5: Total System Jitter Budget for 2.5 GT/s Signaling

Jitter Contribution	Min Rj (ps)	Max Dj (ps)	Tj at BER 10 ⁻¹² (ps) (Note 1, Note 3)	Tj at BER 10 ⁻⁶ (ps) (Note 2)
Tx	2.8	60.6	100	87
Ref Clock	4.7	41.9	108	86
Media	0	90	90	90
Rx	2.8	120.6	160	147
Linear Total Tj:			458	410
Root Sum Square (RSS) Total Tj:			399.13	371.52

Notes:

1. RSS equation for BER 10⁻¹² Tj = $\sum Dj_n + 14.069 * \sqrt{\sum Rj_n^2}$
2. RSS equation for BER 10⁻⁶ Tj = $\sum Dj_n + 9.507 * \sqrt{\sum Rj_n^2}$
3. This column provides jitter limits at different BER values on a bathtub curve. If bathtub curves are not used in jitter measurements, then the jitter limit in the 10⁻⁶ column must be used as the total jitter limit for measurements using approximately 10⁶ unit intervals of data.

Table 4-6: Allocation of Interconnect Jitter Budget for 2.5 GT/s Signaling

Jitter Parameter	Jitter Budget Value (UI)		Comments
PCI Express Add-in Card	$J_{AR} < 0.0575$	$J_{AT} < 0.0650$	Notes 1, 2
System Board and Connector	$J_{ST} < 0.1675$	$J_{SR} < 0.1600$	Notes 1, 3
Total Jitter	$J_T < 0.225$		Note 1

Notes:

1. All values are referenced to 100 Ω , realized as two 50 Ω resistances. The jitter budget values include all possible crosstalk impacts (near-end and far-end) and potential mismatch of the actual interconnect with respect to the 100 Ω reference load. The *PCI Express Base Specification* allows an interconnect jitter budget of 0.225 UI (equivalent to 90 ps for a 400 ps Unit-Interval). The allocated jitter budget values in Table 4-5 and Table 4-6 directly correlate to the eye diagram widths in Section 4.8. Tradeoffs in terms of attenuation, crosstalk, and mismatch can be made within the budget allocations specified. No additional guard band is specifically allocated.
2. The jitter allocations are then assumed per differential pair per the table. These allocation assumptions must also include any effects of far-end crosstalk. The Add-in Card budget does not include the Add-in Card edge-finger or connector. However, it does include potential jitter from the AC coupling capacitors on the Transmitter (TX) interconnect of the Add-in Card. The budget allocations generally allow for a maximum of 4-inch trace lengths for differential pairs having an approximate 0.127 mm (5 mil) trace width. No specific trace geometry, however, is explicitly defined in this specification. The subscripts of the symbol designators, T and R, represent the Transmitter and Receiver respectively.
3. The system board budget includes the PCI Express connector and assumes it is mated with the card edge-finger. Refer to Section 6.3 for specifics on the standalone connector budget. The system board budget includes potential jitter from the AC coupling capacitors on the Transmitter (TX) interconnect on the system board. The subscripts of the symbol designators, T and R, represent the Transmitter and Receiver respectively.

The total system jitter budget for 5.0 GT/s signaling specifies separate Rj and Dj limits for each of the four components in the jitter budget (see Table 4-7). Refer to the *PCI Express Base Specification* for a more detailed discussion of the system jitter budget, Rj and Dj.

Table 4-7: Total System Jitter Budget for 5.0 GT/s Signaling

Jitter Contribution	Max RMS Rj (ps)	Max Dj (ps)	Tj at BER 10 ⁻¹² (ps) (Note 1)
Tx	1.4	30	50
Ref Clock	3.1	0	43.6
Media	0	58	58
Rx	1.4	60	80
Linear Total Tj:			231.6
Root Sum Square (RSS) Total Tj:			200

Notes:

1. RSS equation for BER 10⁻¹² Tj = $\sum Dj_n + 14.069 * \sqrt{\sum Rj_n^2}$

The total system jitter budget for 8.0 GT/s and higher data rates signaling does not set separate Rj and Dj limits for all four components in the jitter budget. Refer to the *PCI Express Base Specification*, for a more detailed discussion of the system jitter budget at 8.0 GT/s and higher data rates.

The jitter budget distributions above are used to derive the eye diagram widths as described later in this chapter. However, they are provided here only as a design guideline. Compliance measurements must be verified against the eye diagrams themselves as defined in Section 4.8.

4.7.4. Crosstalk

Add-in Cards must ensure they can pass Transmitter Path and Receiver Path Eye Diagram requirements at the highest data rate supported and all lower data rates. Crosstalk is included directly or indirectly in these tests. See the following sections for specific information:

- 4.8.1, Add-in Card Transmitter Path Compliance Eye Diagram at 2.5 GT/s
- 4.8.2, Add-in Card Transmitter Path Compliance Eye Diagrams at 5.0 GT/s
- 4.8.3, Add-in Card Transmitter Path Compliance Eye Diagrams at 8.0 GT/s
- 4.8.4, Add-in Card Transmitter Path Compliance Eye Diagrams at 16.0 GT/s
- 4.8.5, Add-in Card Transmitter Path Compliance Eye Diagrams at 32.0 GT/s
- 4.8.6, Add-in Card Transmitter Path Pulse Width Jitter at 16.0 GT/s
- 4.8.7, Add-in Card Transmitter Path Pulse Width Jitter at 32.0 GT/s
- 4.8.8, Add-in Card Minimum Receiver Path Sensitivity Requirements at 2.5 GT/s
- 4.8.9, Add-in Card Minimum Receiver Path Sensitivity Requirements at 5.0 GT/s
- 4.8.10, Add-in Card Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s
- 4.8.11, Add-in Card Minimum Receiver Path Sensitivity Requirements at 16.0 GT/s
- 4.8.12, Add-in Card Minimum Receiver Path Sensitivity Requirements at 32.0 GT/s

System boards must ensure they can pass Transmitter Path and Receiver Path Eye Diagram requirements at at the highest data rate supported and all lower data rates. Crosstalk is included directly or indirectly in these tests. See the following sections for specific information:

- 4.8.13, System Board Transmitter Path Compliance Eye Diagram at 2.5 GT/s
- 4.8.14, System Board Transmitter Path Compliance Eye Diagram at 5.0 GT/s
- 4.8.15, System Board Transmitter Path Compliance Eye Diagram at 8.0 GT/s
- 4.8.16, System Board Transmitter Path Compliance Eye Diagram at 16.0 GT/s
- 4.8.17, System Board Transmitter Path Compliance Eye Diagram at 32.0 GT/s
- 4.8.18, System Board Minimum Receiver Path Sensitivity Requirements at 2.5 GT/s
- 4.8.19, System Board Minimum Receiver Path Sensitivity Requirements at 5.0 GT/s
- 4.8.20, System Board Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s
- 4.8.21, System Board Minimum Receiver Path Sensitivity Requirements at 16.0 GT/s
- 4.8.22, System Board Minimum Receiver Path Sensitivity Requirements at 32.0 GT/s

4.7.5. Lane-to-Lane Skew

The skew at any point is measured using zero crossings of differential voltage of the compliance pattern, while simultaneously transmitting on all physical Lanes (see Table 4-8). The compliance pattern is defined in the *PCI Express Base Specification*.

Table 4-8: Allowable Interconnect Lane-to-Lane Skew

Skew Parameter	Symbol	Skew Values	Comments
Total Interconnect Skew	S_T	1.6 ns	This does not include Transmitter output skew, $L_{TX-SKEW}$ (specified in the <i>PCI Express Base Specification</i>). The total skew at the Receiver ($S_T + L_{TX-SKEW}$) is smaller than $L_{RX-SKEW}$ (specified in the <i>PCI Express Base Specification</i>) to minimize latency for this Add-in Card topology.
PCI Express Add-in Card	S_A	0.35 ns	Estimates about a 2-inch trace length delta on FR-4 boards.
System Board	S_S	1.25 ns	Estimates about a 7-inch trace length delta on FR-4 boards.

4.7.6. Transmitter De-emphasis and Equalization

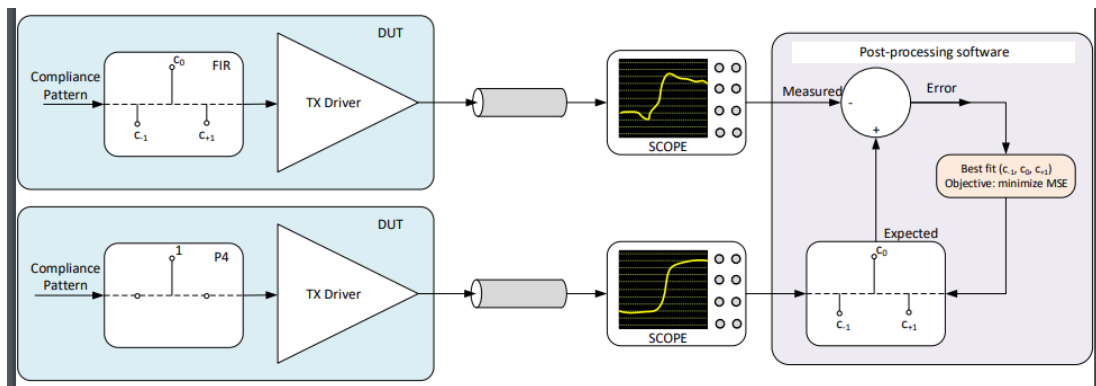
De-emphasis is required for Add-in Cards and system boards to reduce ISI. For 5.0 GT/s and lower data rates, refer to the *PCI Express Base Specification* for de-emphasis requirements. For 8.0 GT/s and higher data rates, refer to the *PCI Express Base Specification* for equalization preset requirements. For implementation details, refer to the *PCI Express Base Specification*. A motherboard must meet eye diagram requirements defined in the *PCI Express Base Specification* at 8.0 GT/s and higher data rates on each lane with one or more preset equalization settings.



IMPLEMENTATION NOTE

Preset Test Requirements at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s

All Add-in Cards and system boards operating at 8.0 GT/s and 16.0 GT/s are required to meet the preset test as described in the *PCI Express Base Specification*. The test consists of acquiring the Tx compliance waveforms from the device under test for each preset then analyzing the waveforms together to confirm that the preset requirements have been met. For 32.0 GT/s, post-processing for Preset test will be done differently than defined in the *PCI Express Base Specification*, using AC fitting method (see Figure 4-6).



Note: Difference between best fit ($c-1$, c_0 , $c+1$) coefficients and expected coefficients is used to compute equalization errors for pre-emphasis, de-emphasis, boost, and Voltage swing

Figure 4-6. TX Equalization Based on AC Fit Method

A system board shall meet the following additional rules for this specification:

- The system board initial TX preset at 8.0 GT/s shall be P1, P7, or P8, unless the next point applies.
- If the equivalent of the $ps21_{TX}$ parameter defined in the *PCI Express Base Specification*, measured at data rates of 8.0 GT/s at the end of the 8.0 GT/s System-Board Test Channel without de-embedding shows a loss of more than 12 dB, then the system board initial TX preset at 8.0 GT/s shall be P7 or P8. The system board initial TX preset at 16.0 GT/s shall be P7 if the Add-in Card does not request an initial preset.
- The system board initial TX preset at 32.0 GT/s shall be P5 if the Add-in Card does not request an initial preset.

An Add-in Card shall meet the following additional rules for this specification:

- If the system board loss is less than 12 dB the Add-in Card shall receive with a BER of less than 10^{-4} at 8.0 GT/s with presets P1, P7, and P8.
- If the system board loss is more than 12 dB, the Add-in Card shall receive with a BER of less than 10^{-4} at 8.0 GT/s with presets P7 and P8.
- The Add-in Card shall receive with a BER of less than 10^{-4} at 16.0 GT/s with preset P7 if it does not request a specific initial preset at 16.0 GT/s. If the Add-in Card does request an initial preset at 16.0 GT/s it must be able to receive with a BER of less than 10^{-4} at the request preset.
- The Add-in Card shall receive with a BER of less than 10^{-4} at 32.0 GT/s with preset P5 if it does not request a specific initial preset at 32.0 GT/s. If the Add-in Card does request an initial preset at 32.0 GT/s it must be able to receive with a BER of less than 10^{-4} at the requested preset.

4.7.7. Skew within the Differential Pair

The skew within the differential pair gives rise to a common-mode signal component, which can, in turn, increase Electromagnetic Interference (EMI). The differential pair shall be routed such that the skew within differential pairs is less than 0.064 mm (2.5 mil) for the Add-in Card and 0.127 mm (5 mil) for the system board.

4.7.8. Differential Data Trace Impedance

The PCB trace pair differential impedance for a 5.0 GT/s capable data pair must be in the range of 68 Ω to 105 Ω . The PCB trace pair differential impedance for an 8.0 GT/s capable data pair must be in the range of 70 Ω to 100 Ω . The PCB trace pair differential impedance for 16.0 GT/s and higher data rate capable data pair must be in the range of 72.5 Ω to 97.5 Ω . These limits apply to both the Add-in Card and the system board.



IMPLEMENTATION NOTE

Differential PCB Trace Impedance

The PCB trace impedance requirement specified in Section 4.7.8 only applies to topologies that support 5.0 GT/s, 8.0 GT/s, 16.0 GT/s, or 32.0 GT/s covered by this form factor specification that use the connector defined in this form factor specification.

Specifically, the *PCI Express Card Electromechanical Specification* covers the following two topologies (as defined in Section 4.6.1):

- PCI Express devices across one card electromechanical connector on a system board and an Add-in Card.
- PCI Express devices across two card electromechanical connectors on a system board, a riser card, and an Add-in Card, where the connector between the riser card and the Add-in Card is a card electromechanical connector.

Motherboards with lossy or reflective channels may need to have tighter impedance control.

Designers should attempt to minimize the impedance discontinuities from vias, the connectors, package traces, cables, and other similar structures.

Furthermore, designers should follow the Add-in Card and system board layout requirements and recommendations as described in Sections 11.2 and 11.3 when developing devices that operate at 16.0 GT/s or higher data rates.

Other topologies governed by different specifications may impose different impedance requirements or leave the impedance unspecified.

For example, the topology of “PCI Express devices on the same system board” does not fit within a form factor specification and hence must only follow the requirements of the *PCI Express Base Specification*. The *PCI Express Base Specification* does not define a PCB trace impedance requirement so with this topology designers can choose the PCB trace impedance that is best for their applications.

This specification does not define a PCB trace impedance requirement for a 2.5 GT/s capable data pair, so for a system board or Add-in Card that only supports 2.5 GT/s, designers can choose the PCB trace impedance that is best for their applications.

4.7.9. Differential Data Trace Propagation Delay

The propagation delay for an Add-in Card data trace from the edge-finger to the Receiver/Transmitter must not exceed 750 ps.

4.7.10. Add-in Card Insertion Loss Limit for 16.0 GT/s

The insertion loss from the top of the edge-finger to the silicon die pad must not exceed -8.0 dB at 8 GHz. This requirement applies to both the transmitter and receiver interconnect and the total loss includes PCB insertion loss, vias (if any), AC Capacitors (applicable to transmitter interconnect), and silicon package including the effective die capacitance.

4.7.11. Add-in Card Insertion Loss Limit for 32.0 GT/s

The insertion loss from the top of the edge-finger to the silicon die pad must not exceed -9.5 dB at 16 GHz. This requirement applies to both the transmitter and receiver interconnect and the total loss includes PCB insertion loss, vias (if any), AC Capacitors (applicable to transmitter interconnect), and silicon package including the effective die capacitance.

4.8. Eye Diagrams at the Connector Interface

The eye diagrams defined in this section represent the compliance eye diagrams that must be met for both the Add-in Card and a system board interfacing with such an Add-in Card. The specific measurement requirements (probe test points, calibrated system board specifics, etc.) for compliance of physical components are specified in the *PCI Express Architecture PHY Test Specification*. A minimum sample size of 1×10^6 UI is required for the eye diagram measurements at data rates of 2.5 GT/s and 5.0 GT/s. A minimum sample size of 1.5×10^6 UI is required at 8.0 GT/s. A minimum sample size of 2.0×10^6 UI is required at 16.0 GT/s and 32.0 GT/s. These compliance eye diagrams with BER of 10^{-12} can also be used for simulation by following the guidelines explained in Section 4.7. The eye diagrams specified for 5.0 GT/s include de-emphasis jitter effects. De-emphasis jitter is not derated in 5.0 GT/s measurements.

4.8.1. Add-in Card Transmitter Path Compliance Eye Diagram at 2.5 GT/s

The eye diagrams for the Add-in Card's Transmitter path compliance at 2.5 GT/s are defined in Table 4-9 and Figure 4-7.

Table 4-9: Add-in Card Transmitter Path Compliance Eye Requirements at 2.5 GT/s

Parameter	Min	Max	Unit	Comments
V_{TXA}	514	1200	mV	Notes 1, 2, 5
V_{TXA_d}	360	1200	mV	Notes 1, 2, 5
T_{TXA}	287		ps	Notes 1, 3, 5
$T_{TXA-MEDIAN-to-MAX-JITTER}$		56.5	ps	Notes 1, 4, 5

Notes:

1. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 8b/10b (refer to the *PCI Express Base Specification*) is being transmitted during the test.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.
3. T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 10^6 UI. This value can be reduced to 274 ps for simulation purpose at BER 10^{-12} .
4. $T_{TXA-MEDIAN-to-MAX-JITTER}$ is the maximum time delta between the jitter median and the maximum deviation from the median. The sample size for this measurement is 10^6 UI. This value can be increased to 63 ps for simulation purpose at BER 10^{-12} .
5. The values in this table are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the Add-in Card (see Figure A-1). The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PCI Express Architecture, PHY Test Specification*.

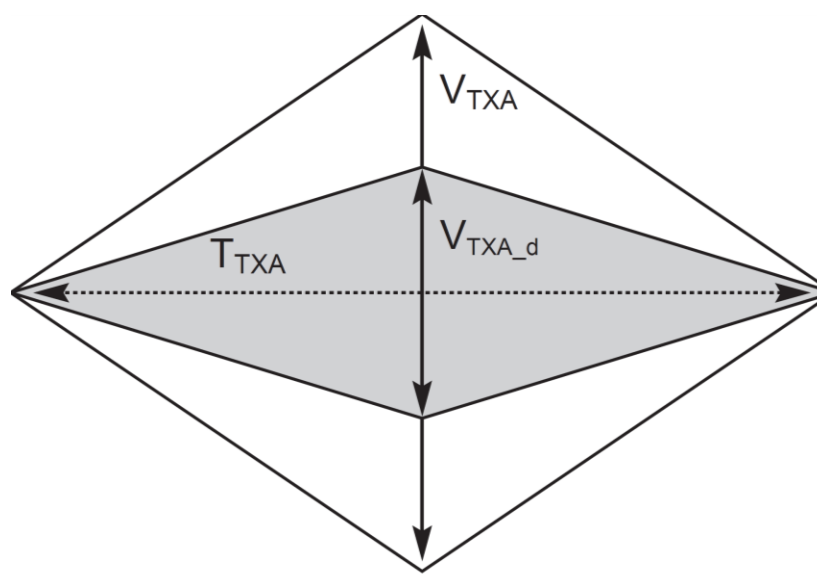


Figure 4-7: Add-in Card Transmitter Path Compliance Eye Diagram

4.8.2. Add-in Card Transmitter Path Compliance Eye Diagrams at 5.0 GT/s

The eye diagrams for the Add-in Card's Transmitter path compliance at 5.0 GT/s are defined in Table 4-10, Table 4-11, Table 4-12, and Table 4-13. See Figure 4-7 for the Add-in Card transmitter path compliance eye diagram.

Table 4-10: Add-in Card Transmitter Path Compliance Eye Requirements for 5.0 GT/s at 3.5 dB De-emphasis

Parameter	Min	Max	Unit	Comments
V_{TXA}	380	1200	mV	Notes 1, 2, 4
V_{TXA_d}	380	1200	mV	Notes 1, 2, 4
T_{TXA} (with crosstalk)	123		ps	Notes 1, 3, 4
T_{TXA} (without crosstalk)	126		ps	

Notes:

1. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that compliance pattern with 8b/10b encoding (refer to the *PCI Express Base Specification*) is being transmitted during the test.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.
3. T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 10^6 UI. This calculated eye width at BER 10^{-12} to meet or exceed T_{TXA} . If the Add-in Card uses non-interleaved routing, then crosstalk will be present in the measured data. If the Add-in Card uses interleaved routing, then crosstalk is not present, and an adjusted minimum eye width is used.
4. The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express connector. This channel shall be referenced as the 5.0 GT/s Add-in Card Test Channel. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PCI Express Architecture PHY Test Specification*.

The Add-in Card total jitter for the Transmitter and the Transmitter interconnect must meet the requirements in Table 4-11 when decomposed into random and deterministic jitter.

Table 4-11: Add-in Card Jitter Requirements for 5.0 GT/s Signaling at 3.5 dB De-emphasis

	Max Rj (ps RMS)	Max Dj (ps)	Tj at BER 10^{-12} (ps)
With crosstalk	1.4	57	77
Without crosstalk	1.4	54	74

Table 4-12: Add-in Card Transmitter Path Compliance Eye Requirements for 5.0 GT/s at 6.0 dB De-emphasis

Parameter	Min	Max	Unit	Comments
V_{TXA}	306	1200	mV	Notes 1, 2, 4
V_{TXA_d}	260	1200	mV	Notes 1, 2, 4
T_{TXA} (With crosstalk)	123		ps	Notes 1, 3, 4
T_{TXA} (Without crosstalk)	126		ps	

Notes:

1. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that compliance pattern with 8b/10b encoding (refer to the *PCI Express Base Specification*) is being transmitted during the test.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.
3. T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA} . If the Add-in Card uses non-interleaved routing, then crosstalk will be present in the measured data. If the Add-in Card uses interleaved routing, then crosstalk will not be present, and an adjusted minimum eye width is used.
4. The values in this table are measured using the 5.0 GT/s Add-in Card Test Channel. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PCI Express Architecture PHY Test Specification*.

The Add-in Card total jitter for the Transmitter and the Transmitter interconnect must meet the requirements in Table 4-13 when decomposed into random and deterministic jitter.

Table 4-13: Add-in Card Jitter Requirements for 5.0 GT/s Signaling at 6.0 dB De-emphasis

	Max Rj (ps RMS)	Max Dj (ps)	Tj at BER 10^{-12} (ps)
With crosstalk	1.4	57	77
Without crosstalk	1.4	54	74

4.8.3. Add-in Card Transmitter Path Compliance Eye Diagrams at 8.0 GT/s

The eye diagrams for the Add-in Card's Transmitter path compliance at 8.0 GT/s are defined in Table 4-14. The Add-in Card shall pass the eye diagram requirements with at least one of the TX equalization presets defined in the *PCI Express Base Specification*. The eye diagram requirements are evaluated after the behavioral CDR and the behavioral RX Equalization Algorithm defined in the *PCI Express Base Specification* are applied.

Table 4-14: Add-in Card Transmitter Path Compliance Eye Requirements at 8.0 GT/s

Parameter	Min	Max	Unit	Comments
V_{TXA}	34	1300	mV	Notes 1, 2, 4
V_{TXA_d}	34	1300	mV	Notes 1, 2, 4
T_{TXA}	41.25		ps	Notes 1, 3, 4

Notes:

1. A worst-case reference clock with 1 ps RMS jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the *PCI Express Base Specification*) is being transmitted during the test.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12} . For lab use, an informative voltage limit (V_{TXA} and V_{TXA_d}) at a BER of 10^{-6} is 46 mV.
3. T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA} .
4. The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of approximately four inches of 85 Ω trace, followed by a second PCI Express connector, followed by approximately 10.8 inches of 85 Ω trace, followed by a reference receiver package all behind a standard PCI Express connector. This channel shall be referenced as the 8.0 GT/s Add-in Card Test Channel. S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant motherboard.

4.8.4. Add-in Card Transmitter Path Compliance Eye Diagrams at 16.0 GT/s

The eye diagrams for the Add-in Card's Transmitter path compliance at 16.0 GT/s are defined in Table 4-15. The Add-in Card shall pass the eye diagram requirements with at least one of the TX equalization presets defined in the *PCI Express Base Specification*. The eye diagram requirements are evaluated after the behavioral CDR and the behavioral RX Equalization Algorithm defined in the *PCI Express Base Specification*, are applied.

Table 4-15: Add-in Card Transmitter Path Compliance Eye Requirements at 16.0 GT/s

Parameter	Min	Max	Unit	Comments
V_{TXA}	23.0	1300	mV	Notes 1, 2, 4
V_{TXA_d}	23.0	1300	mV	Notes 1, 2, 4
T_{TXA}	24.75		ps	Notes 1, 3, 4

Notes:

1. A worst-case reference clock with 0.7 ps RMS jitter at the receiver of the Add-in Card is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the *PCI Express Base Specification*) is being transmitted during the test.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12} .
3. T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 2×10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA} .
4. The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 85 Ω FR-4 trace with an insertion loss of 14 dB at Nyquist, followed by a root reference package all behind a standard PCI Express connector. This channel shall be referenced as the 16.0 GT/s Add-in Card Test Channel. S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant motherboard.

4.8.5. Add-in Card Transmitter Path Compliance Eye Diagrams at 32.0 GT/s

The eye diagrams for the Add-in Card's Transmitter path compliance at 32.0 GT/s are defined in Table 4-16. The Add-in Card shall pass the eye diagram requirements with at least one of the TX equalization presets defined in the *PCI Express Base Specification*. The eye diagram requirements are evaluated after the behavioral CDR and the behavioral RX Equalization Algorithm defined in the *PCI Express Base Specification*, are applied.

Table 4-16: Add-in Card Transmitter Path Compliance Eye Requirements at 32.0 GT/s

Parameter	Min	Max	Unit	Comments
V_{TXA}	22	1300	mV	Notes 1, 2, 4
T_{TXA}	10.625		ps	Notes 1, 3, 4

Notes:

1. A worst-case reference clock with 0.25 ps RMS jitter at the receiver of the Add-in Card is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the *PCI Express Base Specification*) is being transmitted during the test. The eye limits in this Table are different than *PCIe Express Base Specification* to account for system board crosstalk that is not present during measurement.
2. V_{TXA} is the minimum differential peak-peak output voltage. The voltage measurements are done at a BER of 10^{-12} .
3. T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 2×10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA} .
4. The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 85 Ω trace with an insertion loss of 18 dB at 16 GHz, followed by a root reference package all behind a standard PCI Express connector. This channel shall be referenced as the 32.0 GT/s Add-in Card Test Channel. S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant motherboard.

4.8.6. Add-in Card Transmitter Path Pulse Width Jitter at 16.0 GT/s

The Uncorrelated Total and Deterministic Pulse Width Jitter ($T_{TX-UPW-TJ}$ and $T_{TX-UPW-DJDD}$) at a BER of 10^{-12} are defined in Table 4-17. The Add-in Card shall pass the timing requirements with the Jitter Measurement Pattern defined in the *PCI Express Base Specification*. The pulse width jitter requirements are evaluated after the -12 dB CTLE curve from the behavioral reference equalizer defined in the *PCI Express Base Specification*, is applied.

Table 4-17: Add-in Card Transmitter Path Uncorrelated Pulse Width Jitter Requirements at 16.0 GT/s

Parameter	Min	Max	Unit	Comments
$T_{TX-UPW-TJ}$	0	12.5	ps PP @ BER 10^{-12}	
$T_{TX-UPW-DJDD}$	0	5.0	ps PP @ BER 10^{-12}	

4.8.7. Add-in Card Transmitter Path Pulse Width Jitter at 32.0 GT/s

The Uncorrelated Total and Deterministic Pulse Width Jitter ($T_{TX-UPW-TJ}$ and $T_{TX-UPW-DJDD}$) at a BER of 10^{-12} are defined in Table 4-18. The Add-in Card shall pass the timing requirements with the Jitter Measurement Pattern defined in the *PCI Express Base Specification*. The pulse width jitter requirements are evaluated after the optimal CTLE curve ranging from -5 dB to -15 dB from the behavioral reference equalizer defined in the *PCI Express Base Specification*, is applied.

Table 4-18: Add-in Card Transmitter Path Uncorrelated Pulse Width Jitter Requirements at 32.0 GT/s

Parameter	Min	Max	Unit	Comments
$T_{TX-UPW-TJ}$	0	6.25	ps PP @ BER 10^{-12}	
$T_{TX-UPW-DJDD}$	0	2.5	ps PP @ BER 10^{-12}	

4.8.8. Add-in Card Minimum Receiver Path Sensitivity Requirements at 2.5 GT/s

The minimum sensitivity values for the Add-in Card's Receiver path compliance at 2.5 GT/s are defined in Table 4-19, and a representative eye diagram is shown in Figure 4-8.

Table 4-19: Add-in Card Minimum Receiver Path Sensitivity Requirements at 2.5 GT/s

Parameter	Min	Max	Unit	Comments
V_{RXA}	238	1200	mV	Notes 1, 2, 5
V_{RXA_d}	219	1200	mV	Notes 1, 2, 5
T_{RXA}	246		ps	Notes 1, 3, 5
$T_{RXA-MEDIAN-to-MAX-JITTER}$	77		ps	Notes 1, 4, 5

Notes:

1. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. Compliance pattern is used when the receiver test is run.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{RXA_d}). V_{RXA} and V_{RXA_d} are differential peak-peak output voltages.
3. T_{RXA} is the eye width. The sample size for this measurement is required to be at least 10^6 UI. This value can be reduced to 233 ps for simulation purpose at BER 10^{-12} .
4. $T_{RXA-MEDIAN-to-MAX-JITTER}$ is the maximum time delta between the jitter median and the maximum deviation from the median. The sample size for this measurement is 10^6 UI. This value can be increased to 83.5 ps for simulation purpose at BER 10^{-12} .
5. The values in this table are initially referenced to an ideal 100 Ω differential load. The resultant values, when provided to the Receiver interconnect path of the Add-in Card, allow for a demonstration of compliance of the overall Add-in Card Receiver path. The sensitivity requirements are defined and centered with respect to the jitter median. Exact conditions required for verifying compliance against these values are given in the *PCI Express Architecture PHY Test Specification*.

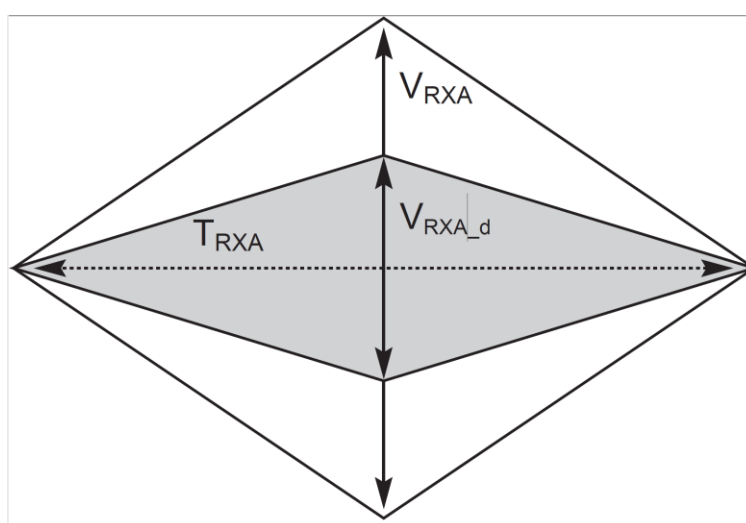


Figure 4-8: Representative Composite Eye Diagram for Add-in Card Receiver Path Compliance

4.8.9. Add-in Card Minimum Receiver Path Sensitivity Requirements at 5.0 GT/s

The minimum sensitivity values for the Add-in Card's Receiver path compliance at 5.0 GT/s are defined in Table 4-20, and a representative eye diagram is shown in Figure 4-8.

Table 4-20: Add-in Card Minimum Receiver Path Sensitivity Requirements at 5.0 GT/s

Parameter	Min	Max	Unit	Comments
V_{RXA}	225	1200	mV	Notes 1, 2, 3
V_{RXA_d}	225	1200	mV	Notes 1, 2, 3
1.5 – 100 MHz RMS Jitter	3.4		ps RMS	
33 kHz REFCLK Residual	75		ps PP	
< 1.5 MHz RMS Jitter	4.2		ps RMS	
1.5 – 100 MHz Dj	30		ps PP	
> 100 MHz Dj	27		ps PP	

Notes:

1. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. Compliance pattern is used when the receiver test is run.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{RXA_d}). V_{RXA} and V_{RXA_d} are differential peak-peak output voltages.
3. The values in this table are initially calibrated with a reference channel consisting of a 5.0 GT/s Add-in Card Test Channel followed by a 5.0 GT/s System-Board Test Channel. After reference calibration, the 5.0 GT/s System-Board Test Channel is removed and the Add-in Card to be tested is placed into a standard PCI Express connector. The resultant values, when provided to the Receiver interconnect path of the Add-in Card, allow for a demonstration of compliance of the overall Add-in Card Receiver path. The exact setup and methodology for injecting this signal into the Receiver interconnect path of the Add-in Card are not specified. The values in this table may need to be adjusted based on the exact test setup and methodology. For example, if the impedance of the test setup does not create the worst-case mismatch that could be present with a real system board or the test setup does not provide crosstalk (only a single Lane is tested, etc.) the values in this table must be adjusted accordingly.

4.8.10. Add-in Card Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s

The minimum sensitivity values for the Add-in Card's Receiver path compliance at 8.0 GT/s are defined in Table 4-21 and Table 4-22. The receiver path shall be tested with a worst-case eye to verify that it achieves a $BER < 10^{-12}$. This worst-case eye is calibrated using TX equalization settings that are optimal with the reference equalizer for each calibration channel. After calibration, the test-generator's TX equalization may be adjusted using the transmitter equalization setting in the required TX equalization space preferred by the device under test, without changing any other parameter of the test signal or recalibrating the test signal.

If the test generator's TX equalization settings are adjusted away from the optimal settings and the test generator is not able to change transmitter equalization without impacting other calibrated parameters – then the other parameters must be adjusted back to the specified values.

If the test is not run in a way that produces the worst-case Crosstalk that would be present with all lanes active, the additional Crosstalk must be accounted for in some other way. The test is performed with two different test channels, a long test channel and a short test channel. While the receiver's capacity to adapt its own equalization is part of the test, its ability to request the link partner's transmitter to change its transmitter equalization is tested by applying a signal whose equalization level is suboptimal compared to the jitter sensitivity test signal described above. For this signal, the reference receiver would not be able to achieve proper equalization by means of its own CTLE and DFE alone. Such a signal can be defined using the signal resulting from the calibration method described above and adjusting the test-generator equalization. If the RX under test is more capable than the reference (CTLE+DFE) receiver, the RX under test may not require the TX to change its equalization levels to achieve a $BER < 10^{-12}$. In any case, equalization settings resulting from this procedure must be used for the RX test and if the RX requires the TX equalization to change, such change must be accommodated by the test set-up used.

A specific methodology for this procedure is outside the scope of this specification. Refer to compliance program test procedures for specific test equipment for specific methodology details.

Table 4-21: Long Channel Add-in Card Min Receiver Path Sensitivity Requirements at 8.0 GT/s

Parameter	Min	Max	Unit	Comments
$V_{RX-EH-8G}$ Eye Height	34	34	mV	Notes 1, 2, 4
$T_{RX-EH-8G}$ Eye Width	0.33	0.38	UI	Notes 1, 2
Rj (Random Jitter)	3		ps RMS	Notes 5, 6
Sj (Sinusoidal Jitter) 100 MHz	12.5		ps PP	Note 6
Differential Mode Sinusoidal Interference 2.1 GHz	14		mV PP	Note 3

Notes:

1. An ideal reference clock without jitter is assumed for this specification. The 128/130b compliance pattern must be used during calibration for this test. Modified compliance pattern is used when the receiver test is run. Eye height and width values reference $BER = 10^{-12}$.
2. The values in this table are initially calibrated with a reference channel consisting of an 8.0 GT/s Add-in Card Test Channel followed by 8.0 GT/s System-Board Test Channel at the TX SMP connectors on the System-Board Test Channel. The calibration is done with the same post processing as the System Board 8.0 GT/s TX test. After reference calibration, the 8.0 GT/s System-Board Test Channel is removed and the Add-in Card to be tested is placed into a standard PCI Express connector.
3. Eye height and width are specified after the application of the reference receiver. When the optimization of the reference receiver's CTLE and DFE yields an eye height and/or eye width larger than specified, the value for DM-interference is increased.
4. Eye height limits do not account for limitations in test equipment voltage resolution.
5. Rj is applied over the following range. The low frequency limit may be between 1.5 MHz and 10 MHz, and the upper limit is 1.0 GHz. While the nominal value is specified at 3.0 ps RMS, it may be adjusted to meet the value for $T_{RX-EH-8G}$ Eye Width.
6. Rj and Sj are measured without post-processing filters.

Table 4-22: Short Channel Add-in Card Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s

Parameter	Min	Max	Unit	Comments
V _{RX-EH-8G} Eye Height	N/A	N/A	mV	Notes 1, 2, 5
T _{RX-EH-8G} Eye Width	N/A	N/A	UI	Notes 1, 2, 5
R _j (Random Jitter)	3		ps RMS	Note 4
S _j (Sinusoidal Jitter) 100 MHz	12.5		ps PP	
Differential Mode Sinusoidal Interference 2.1 GHz	14		mV PP	Note 3

Notes:

1. An ideal reference clock without jitter is assumed for this specification. The 128/130b compliance pattern must be used during calibration for this test. Modified compliance pattern is used when the receiver test is run. Eye height and width values refer to a BER = 10^{-12} .
2. The values in this table are initially calibrated with a reference channel consisting of a 8.0 GT/s Add-in Card Test Channel followed by 8.0 GT/s System-Board Test Channel at the TX SMP connectors on the System-Board Test Channel. The calibration is done with the same post processing as the System Board 8.0 GT/s TX test. After reference calibration, the 8.0 GT/s System-board Test Channel is removed and the Add-in Card to be tested is placed into a standard PCI Express connector.
3. Eye height and width are specified after application of the reference receiver. When the optimization of the reference receiver's CTLE and DFE yields an eye height and/or eye width larger than specified, the value for DM-interference is increased.
4. R_j is applied over the following range. The low frequency limit may be between 1.5 MHz and 10 MHz, and the upper limit is 1.0 GHz.
5. For the short channel test, the calibrated test equipment transmitter settings from the long channel test are used. Eye height and eye width are not separately re-calibrated.

4.8.11. Add-in Card Minimum Receiver Path Sensitivity Requirements at 16.0 GT/s

The minimum sensitivity values for the Add-in Card's Receiver path compliance at 16.0 GT/s are defined in Table 4-23. The receiver path shall be tested with a worst-case eye to verify that it achieves a BER < 10^{-12} . This worst-case eye is calibrated using TX equalization settings that are optimal with the reference equalizer for the calibration channel. After calibration, the test-generator's equalization settings may be adjusted using the transmitter equalization setting in the required TX equalization space preferred by the device under test, without changing any other parameter of the test signal or recalibrating the test signal. This adjustment is done through running the PCI Express training protocol.

If the test generator's TX equalization settings are adjusted away from the optimal settings and the test generator is not able to change transmitter equalization without impacting other calibrated parameters – then the other parameters must be adjusted back to the calibrated values.

If the test is not run in a way that produces the worst-case Crosstalk that would be present with all lanes active, the additional Crosstalk must be accounted for in some other way.

Table 4-23. Add-in Card Minimum Receiver Path Sensitivity Requirements at 16.0 GT/s

Parameter	Min	Max	Unit	Comments
V _{RX-EH-16G} Eye Height	15	15	mV	Notes 1, 2, 4
T _{RX-EH-16G} Eye Width	0.3	0.3	UI	Notes 1, 2
Rj (Random Jitter)	1.0		ps RMS	Notes 5, 6
Sj (Sinusoidal Jitter) 100 MHz	6.25		ps PP	Note 6
Differential Mode Sinusoidal Interference 2.1 GHz	14		mV PP	Note 3

Notes:

1. An ideal reference clock without jitter is assumed for this specification. The 128/130b compliance pattern must be used during calibration for this test. Modified compliance pattern is used when the receiver test is run. Eye height and width values refer to BER = 10^{-12} .
2. The values in this table are initially calibrated with a reference channel consisting of a 16.0 GT/s Add-in Card Test Channel followed by a 16.0 GT/s System-Board Test Channel at the TX SMP connectors on the System-Board Test Channel. The calibration is done with the same post processing as the System Board 16.0 GT/s TX test. After reference calibration, the 16.0 GT/s System-Board Test Channel is removed and the add-in card to be tested is placed into a standard PCI Express connector. The end to end CEM calibration channel must meet the requirements (insertion loss and return loss masks) defined for the 16.0 GT/s calibration channel in the *PCI Express Base Specification*.
3. Eye height and width are specified after the application of the reference receiver. V_{RX-EH-16G} and T_{RX-EH-16G} are adjusted following the same process described in the *PCI Express Base Specification* for calibrating the 16.0 GT/s stressed eye test. When the channel insertion loss is varied as part of the 16.0 GT/s stressed eye calibration process the variation must occur in the 16.0 GT/s Add-in Card Test Channel portion of the channel.
4. Eye height limits do not account for limitations in test equipment voltage resolution.
5. Rj is applied over the following range. The low frequency limit may be between 1.5 MHz and 10 MHz, and the upper limit is 1.0 GHz.
6. Rj and Sj are measured without post-processing filters.

4.8.12. Add-in Card Minimum Receiver Path Sensitivity Requirements at 32.0 GT/s

The minimum sensitivity values for the Add-in Card's Receiver path compliance at 32.0 GT/s are defined in Table 4-24. The receiver path shall be tested with a worst-case eye to verify that it achieves a BER < 10^{-12} . This worst-case eye is calibrated using TX equalization settings that are optimal with the reference equalizer for the calibration channel. After calibration, the test-generator's equalization settings may be adjusted using the transmitter equalization setting in the required TX equalization space preferred by the device under test, without changing any other parameter of the test signal or recalibrating the test signal. This adjustment is done through running the PCI Express training protocol.

If the test generator's TX equalization settings are adjusted away from the optimal settings and the test generator is not able to change transmitter equalization without impacting other calibrated parameters – then the other parameters must be adjusted back to the calibrated values.

If the test is not run in a way that produces the worst-case Crosstalk that would be present with all lanes active, the additional Crosstalk must be accounted for in some other way.

Table 4-24. Add-in Card Minimum Receiver Path Sensitivity Requirements at 32.0 GT/s

Parameter	Nominal	Unit	Comments
$V_{RX-EH-32G}$ Eye Height	15	mV	Notes 1, 2, 4, 7
$T_{RX-EW-32G}$ Eye Width	0.3	UI	Notes 1, 2, 7
Rj (Random Jitter)	0.5	ps RMS	Notes 5, 6, 7
Sj (Sinusoidal Jitter) 100 MHz	3.125	ps PP	Note 6, 7
Differential Mode Sinusoidal Interference 2.1 GHz	10	mV PP	Note 3, 7

Notes:

1. An ideal reference clock without jitter is assumed for this specification. The 128/130b compliance pattern must be used during calibration for this test. Modified compliance pattern is used when the receiver test is run. Eye height and width values are calculated at BER of 10^{-12} .
2. The values in this table are initially calibrated with a reference channel consisting of a 32.0 GT/s Add-in Card Test Channel followed by a 32.0 GT/s System-Board Test Channel at the TX MMPX connectors on the System-Board Test Channel. After reference calibration, the 32.0 GT/s System-Board Test Channel is removed and the add-in card to be tested is placed into a standard PCI Express connector. The end to end CEM calibration channel must meet the requirements (insertion loss and return loss masks) defined for the 32.0 GT/s calibration channel in the *PCI Express Base Specification*.
3. Eye height and width are specified after the application of the reference receiver. $V_{RX-EH-32G}$ and $T_{RX-EW-32G}$ are adjusted following the same process described in the PCI Express Base Specification for calibrating the 32.0 GT/s stressed eye test. When the channel insertion loss is varied as part of the 32.0 GT/s stressed eye calibration process the variation must occur in the 32.0 GT/s Add-in Card Test Channel portion of the channel.
4. Eye height limits do not account for limitations in test equipment voltage resolution.
5. Rj is applied over the following range. The low frequency limit may be between 1.5 MHz and 10 MHz, and the upper limit is 1.0 GHz.
6. Rj and Sj are measured without post-processing filters.
7. Refer to *PCI Express Architecture Phy Test Specification* for allowed tolerances around nominal values.

4.8.13. System Board Transmitter Path Compliance Eye Diagram at 2.5 GT/s

The eye diagram for the system board's Transmitter compliance at 2.5 GT/s is defined in Table 4-25 and Figure 4-9.

Table 4-25: System Board Transmitter Path Compliance Eye Requirements at 2.5 GT/s

Parameter	Min	Max	Unit	Comments
V_{TXS}	274	1200	mV	Notes 1, 2, 5
V_{TXS_d}	253	1200	mV	Notes 1, 2, 5
T_{TXS}	246		ps	Notes 1, 3, 5
$T_{TXS-MEDIAN-10-MAX-JITTER}$		77	ps	Notes 1, 4, 5

Notes:

1. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 8b/10b (refer to the *PCI Express Base Specification*) is being transmitted during the test.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.
3. T_{TXS} is the minimum eye width. The sample size for this measurement is required to be at least 10^6 UI. This value can be reduced to 233 ps for simulation purposes at BER 10^{-12} .
4. $T_{TXS-MEDIAN-10-MAX-JITTER}$ is the maximum time delta between the jitter median and the maximum deviation from the median. The sample size for this measurement is 10^6 UI. This value can be increased to 83.5 ps for simulation purpose at BER 10^{-12} .
5. The values in this table are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the Add-in Card when mated with a connector (see Figure A-1). The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PCI Express Architecture PHY Test Specification*.

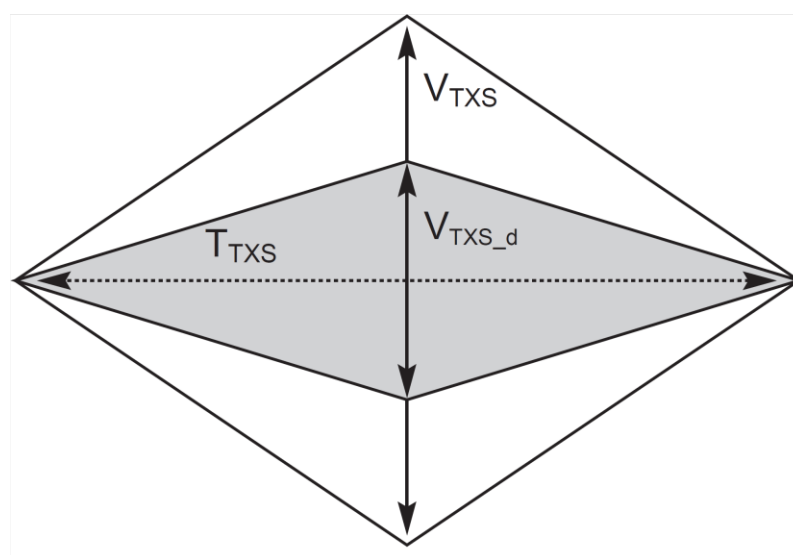
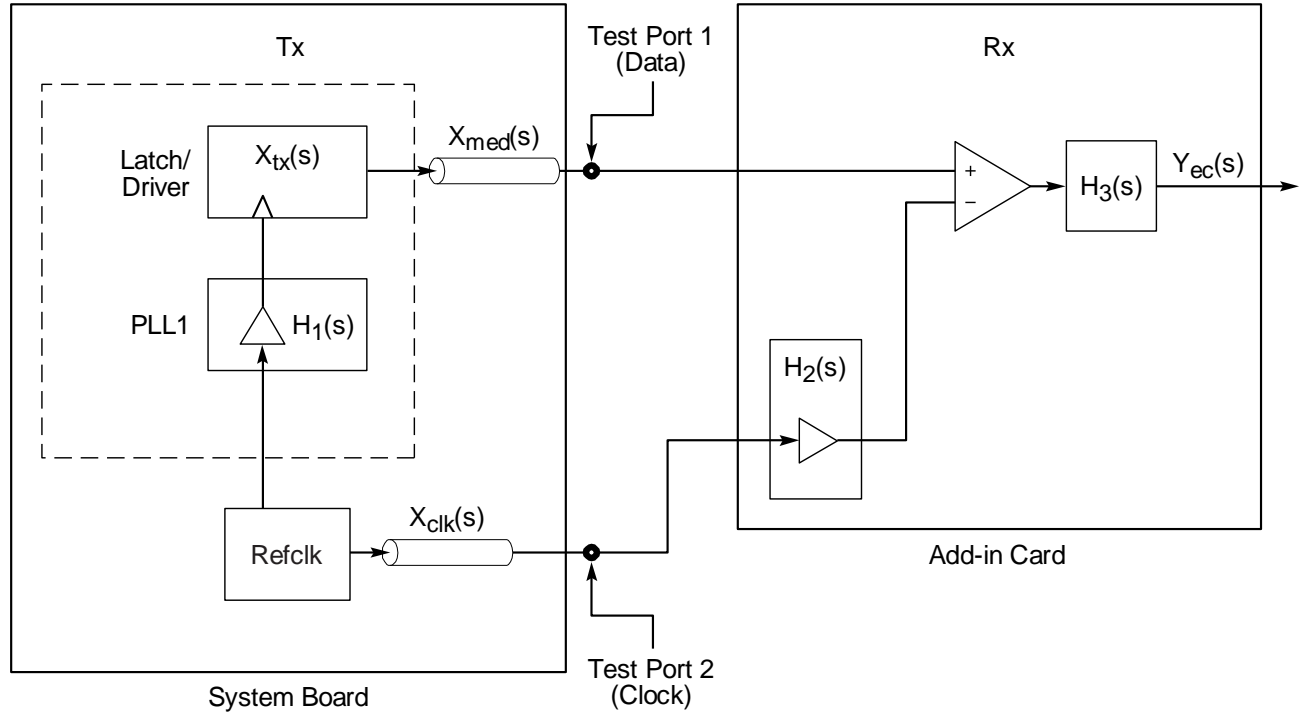


Figure 4-9: System Board Transmitter Path Composite Compliance Eye Diagram

4.8.14. System Board Transmitter Path Compliance Eye Diagram at 5.0 GT/s

The system board Transmitter path measurements at 5.0 GT/s are made using a two-port measurement methodology. Figure 4-9 shows a functional block diagram for a system board and Add-in Card that shows the measurement points for the two-port method.



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Figure 4-10: 5.0 GT/s Two Port Measurement Functional Block Diagram

Equations for the jitter at test port 1 and test port 2 and the eye closure at the Add-in Card Receiver from the test port signals are provided as follows:

Data Port Measurement (Test Port 1):

$$\text{Eq.(1)} \quad X_{dm}(s) = X_{clk}(s)H_1(s)e^{-sT_{d1a}} + X_{tx}(s) + X_{med}(s)$$

Clock Port Measurement (Test Port 2):

$$\text{Eq.(2)} \quad X_{cm}(s) = X_{clk}(s)e^{-sT_{d1b}}$$

Eye Closure at Receiver Due to Signals at Clock and Data Ports:

$$\text{Eq.(3)} \quad Y_{ec}(s) = \{ [X_{clk}(s)H_1(s)e^{-sT_{d1a}} + X_{tx}(s) + X_{med}(s)] - [X_{clk}(s)e^{-sT_{d1b}}][H_2(s)e^{-sT_{d2}}] \} \bullet H_3(s) \\ = (X_{dm}(s) - X_{clk}(s)H_2(s)e^{-sT_{d2}}) \bullet H_3(s)$$

Where $X_{clk}(s)$ is the reference clock transfer function, T_{d1a} is the delay from the reference clock to the data port, T_{d1b} is the delay from the reference clock to the test port, $X_{tx}(s)$ is the driver/latch transfer function, and $X_{med}(s)$ is the interconnect transfer function. Where the RX PLL transfer function $H_2(s)$ and the CDR transfer function $H_3(s)$ are the same as those defined in the *PCI Express Base Specification* with parameters that give rise to the largest eye closure $Y_{ec}(s)$. The delay T_{d2} is swept from -3 ns to $+3$ ns – consistent with the maximum transport delay that can occur in the Add-in Card.

Use the following procedure for the two-port measurement methodology:

1. Gather Data from test port 1 and test port 2 to obtain the spectrum $X_{dm}(s)$ and $X_{cm}(s)$ or equivalent.
2. Calculate the eye closure $Y_{ec}(s)$ or $Y_{ec}(t)$ based on step 3. T_{d2} is swept from -3 ns to $+3$ ns. $H_3(s)$ is defined in the *PCI Express Base Specification*. $H_2(s)$ is one of the following values:

$$H_2(s) = \frac{2\zeta\omega_{n2}s + \omega_{n2}^2}{s^2 + 2\zeta\omega_{n2}s + \omega_{n2}^2}$$

where : $\zeta = 0.54$ (3 dB PK), $\omega_{n2} = 8.61 * 2\pi$ (16MHz 3dB BW) Mrad / s or

$\zeta = 0.54$ (3 dB PK), $\omega_{n2} = 4.31 * 2\pi$ (8 Mhz 3dB BW) Mrad / s or

$\zeta = 1.16$ (1 dB PK), $\omega_{n2} = 1.82 * 2\pi$ (5 MHz 3dB BW) Mrad / s

3. Calculate the eye closure at BER= 10^{-12} based on $Y_{ec}(t)$. The maximum eye closure for any parameters of T_{d2} and $H_2(s)$ in the defined ranges is the total jitter assigned to the system board Transmitter, Transmitter interconnect, and the reference clock.

Table 4-26: System Board Transmitter Path Compliance Eye Requirements at 5.0 GT/s

Parameter	Min	Max	Unit	Comments
V_{TXS}	225	1200	mV	Notes 1, 2, 4
V_{TXS_d}	225	1200		Notes 1, 2, 4
T_{TXS} (with crosstalk)	95		ps	Notes 1, 3, 4
T_{TXS} (without crosstalk)	108		ps	

Notes:

1. All Links are assumed active while generating this eye diagram. The eye diagram requires that compliance pattern with 8b/10b encoding (refer to the *PCI Express Base Specification*) is being transmitted during the test using the de-emphasis level that the system board will use in normal operation.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.
3. T_{TXS} is the minimum eye width. The sample size for the dual port measurement is required to be at least 10^6 UI. The minimum eye opening at BER 10^{-12} is calculated based on the measured data and must meet or exceed T_{TXS} . If the system board uses non-interleaved routing, then crosstalk will be present in the measured data. If the system uses interleaved routing, then crosstalk will not be present, and an adjusted minimum eye width is used.
4. The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated 2-inch 85 Ω differential trace behind a standard PCI express edge-finger. This channel shall be referenced as the 5.0 GT/s System Board Test Channel. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PCI Express Architecture PHY Test Specification*.

The system board total jitter for the transmitter, transmitter interconnect and the reference clock must meet the requirements in Table 4-27 when decomposed into random and deterministic jitter.

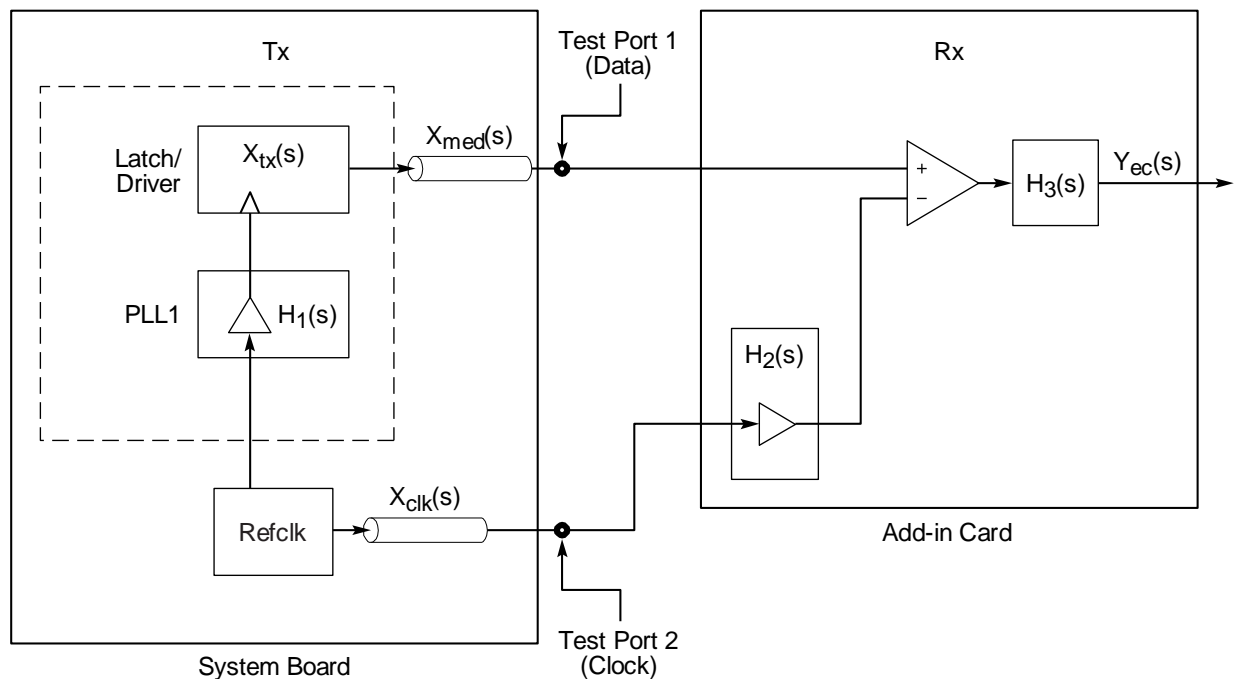
Table 4-27: System Board Jitter Requirements for 5.0 GT/s Signaling

	Max Rj (ps RMS)	Max Dj (ps)	Tj at BER 10^{-12} (ps)
With crosstalk	3.41	57	105
Without crosstalk	3.41	44	92

4.8.15. System Board Transmitter Path Compliance Eye Diagram at 8.0 GT/s

The system board shall pass the eye diagram requirements with at least one of the TX equalization presets defined in the *PCI Express Base Specification*. The eye diagram requirements are evaluated after the behavioral CDR and the behavioral RX Equalization Algorithm defined in the *PCI Express Base Specification*, are applied.

The system board Transmitter path measurements at 8.0 GT/s are made using a two-port measurement methodology. Figure 4-11 shows a functional block diagram for a system board and Add-in Card that shows the measurement points for the two-port method.



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Figure 4-11: 8.0 GT/s Two Port Measurement Functional Block Diagram

Equations for the jitter at test port 1 and test port 2 and the eye closure at the Add-in Card Receiver from the test port signals are provided as follows:

Data Port Measurement (Test Port 1):

$$\text{Eq.(1)} \quad X_{dm}(s) = X_{clk}(s)H_1(s)e^{-sT_{d1a}} + X_{tx}(s) + X_{med}(s)$$

Clock Port Measurement (Test Port 2):

$$\text{Eq.(2)} \quad X_{cm}(s) = X_{clk}(s)e^{-sT_{d1b}}$$

Eye Closure at Receiver Due to Signals at Clock and Data Ports:

$$\begin{aligned} \text{Eq.(3)} \quad Y_{ec}(s) &= \{[X_{clk}(s)H_1(s)e^{-sT_{d1a}} + X_{tx}(s) + X_{med}(s)] - [X_{clk}(s)e^{-sT_{d1b}}][H_2(s)e^{-sT_{d2}}]\} \bullet H_3(s) \\ &= (X_{dm}(s) - X_{clk}(s)H_2(s)e^{-sT_{d2}}) \bullet H_3(s) \end{aligned}$$

Where $X_{clk}(s)$ is the reference clock transfer function, T_{d1a} is the delay from the reference clock to the data port, T_{d1b} is the delay from the reference clock to the test port, $X_{tx}(s)$ is the driver/latch transfer function, and $X_{med}(s)$ is the interconnect transfer function. Where the RX PLL transfer function $H_2(s)$, and CDR transfer function $H_3(s)$ are the same as those defined in the *PCI Express Base Specification* with parameters that give rise to the largest eye closure $Y_{ec}(s)$. The delay T_{d2} is swept from -3 ns to $+3$ ns – consistent with the maximum transport delay that can occur in the Add-in Card.

The two-port measurement methodology is performed according to the following steps:

1. Data is gathered from test port 1 and test port 2 to obtain the spectrum $X_{dm}(s)$ and $X_{cm}(s)$ or equivalent.
2. The eye closure $Y_{ec}(s)$ or $Y_{ec}(t)$ is calculated based on Step 3. T_{d2} is swept from -3 ns to $+3$ ns. $H_3(s)$ is defined in the *PCI Express Base Specification*. $H_2(s)$ is one of the following values:

$$H_2(s) = \frac{2\zeta\omega_{n2}s + \omega_{n2}^2}{s^2 + 2\zeta\omega_{n2}s + \omega_{n2}^2}$$

where: $\zeta = 0.73$ (2 dB PK), $\omega_{n2} = 6.1$ (2 MHz 3dB BW) Mrad / s or

$\zeta = 0.73$ (2 dB PK), $\omega_{n2} = 12.2$ (4 Mhz 3dB BW) Mrad / s or

$\zeta = 1.15$ (1 dB PK), $\omega_{n2} = 11.53$ (5 Mhz 3dB BW) Mrad / s

3. Calculate the eye closure at BER = 10⁻¹² based on $Y_{ec}(t)$. The maximum eye closure for any parameters of T_{d2} and $H_2(s)$ in the defined ranges is the total jitter assigned to the system board Transmitter, Transmitter interconnect, and the reference clock.

Table 4-28: System Board Transmitter Path Compliance Eye Requirements for 8.0 GT/s with Ideal Adaptive TX Equalization

Parameter	Min	Max	Unit	Comments
V_{TXS}	34	1300	mV	Notes 1, 2, 4
V_{TXS_d}	34	1300		Notes 1, 2, 4
T_{TXS}	41.25		ps	Notes 1, 3, 4

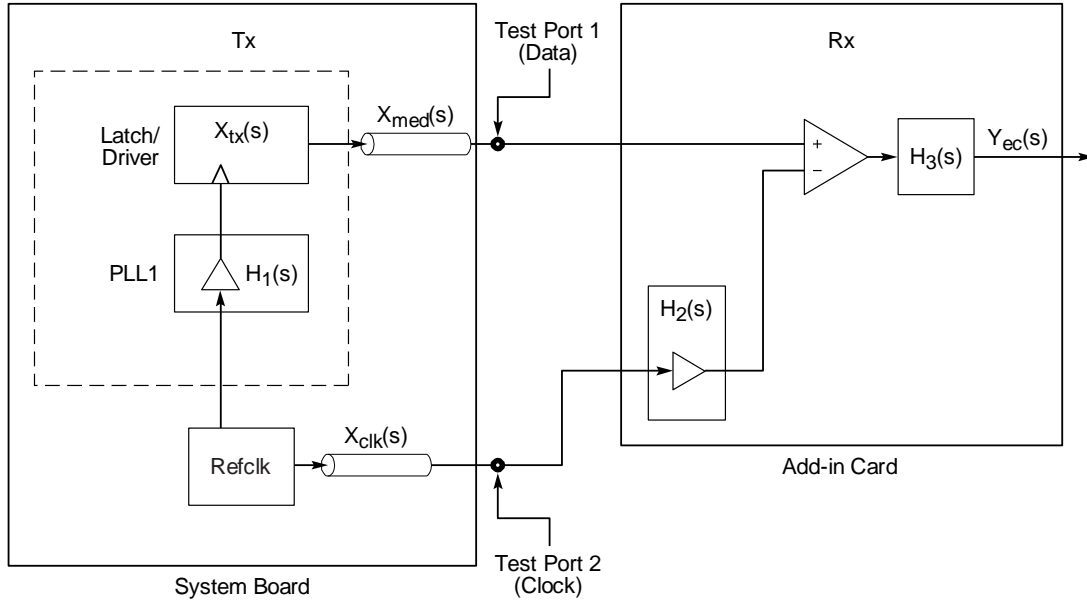
Notes:

1. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the *PCI Express Base Specification*) is being transmitted during the test.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12} . For lab use, an informative voltage limit (V_{TXS} and V_{TXS_d}) at a BER of 10^{-6} is 46 mV.
3. T_{TXS} is the minimum eye width. The sample size for this measurement is required to be least 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXS} .
4. The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 4.0 inches of 85 Ω trace, followed by a reference receiver package behind a standard PCI Express edge-finger. This channel shall be referenced as the 8.0 GT/s System-Board Test Channel. The S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant Add-in Card.

4.8.16. System Board Transmitter Path Compliance Eye Diagram at 16.0 GT/s

The system board shall pass the eye diagram requirements with at least one of the TX equalization presets defined in the *PCI Express Base Specification*. The eye diagram requirements are evaluated after the behavioral CDR and the behavioral RX Equalization Algorithm defined in the *PCI Express Base Specification* are applied.

The system board Transmitter path measurements at 16.0 GT/s are made using a two-port measurement methodology. Figure 4-12 shows a functional block diagram for a system board and Add-in Card that shows the measurement points for the two-port method.



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Figure 4-12: 16.0 GT/s Two Port Measurement Functional Block Diagram

Equations for the jitter at test port 1 and test port 2 and the eye closure at the Add-in Card Receiver from the test port signals are provided as follows:

Data Port Measurement (Test Port 1):

$$\text{Eq.(1)} \quad X_{dm}(s) = X_{clk}(s)H_1(s)e^{-sT_{d1a}} + X_{tx}(s) + X_{med}(s)$$

Clock Port Measurement (Test Port 2):

$$\text{Eq.(2)} \quad X_{cm}(s) = X_{clk}(s)e^{-sT_{d1b}}$$

Eye Closure at Receiver Due to Signals at Clock and Data Ports:

$$\begin{aligned} \text{Eq.(3)} \quad Y_{ec}(s) &= \{ [X_{clk}(s)H_1(s)e^{-sT_{d1a}} + X_{tx}(s) + X_{med}(s)] - [X_{clk}(s)e^{-sT_{d1b}}][H_2(s)e^{-sT_{d2}}] \} \bullet H_3(s) \\ &= (X_{dm}(s) - X_{cm}(s)H_2(s)e^{-sT_{d2}}) \bullet H_3(s) \end{aligned}$$

Where $X_{clk}(s)$ is the reference clock transfer function, T_{d1a} is the delay from the reference clock to the data port, T_{d1b} is the delay from the reference clock to the test port, $X_{tx}(s)$ is the driver/latch transfer function, and $X_{med}(s)$ is the interconnect transfer function. Where the RX PLL transfer function $H_2(s)$, and CDR transfer function $H_3(s)$ are the same as those defined in the *PCI Express Base Specification* with parameters that give rise to the largest eye closure $Y_{ec}(s)$. The delay T_{d2} is swept from -3 ns to $+3$ ns – consistent with the maximum transport delay that can occur in the Add-in Card.

The two-port measurement methodology is performed according to the following steps:

1. Data is gathered from test port 1 and test port 2 to obtain the spectrum $X_{dm}(s)$ and $X_{cm}(s)$ or equivalent.
2. The eye closure $Y_{ec}(s)$ or $Y_{ec}(t)$ is calculated based on equation 3. T_{d2} is swept from -3 ns to +3 ns. $H_3(s)$ is defined in the *PCI Express Base Specification*. $H_2(s)$ is one of the following values:

$$H_2(s) = \frac{2\zeta\omega_{n2}s + \omega_{n2}^2}{s^2 + 2\zeta\omega_{n2}s + \omega_{n2}^2}$$

where: $\zeta = 0.73$ (2 dB PK), $\omega_{n2} = 6.1$ (2 MHz 3dB BW) Mrad / s or

$\zeta = 0.73$ (2 dB PK), $\omega_{n2} = 12.2$ (4 MHz 3dB BW) Mrad / s or

$\zeta = 1.15$ (1 dB PK), $\omega_{n2} = 11.53$ (5 MHz 3dB BW) Mrad / s

3. Calculate the eye closure at $BER = 10^{-12}$ based on $Y_{ec}(t)$. The maximum eye closure for any parameters of T_{d2} and $H_2(s)$ in the defined ranges is the total jitter assigned to the system board Transmitter, Transmitter interconnect, and the reference clock.

Table 4-29: System Board Transmitter Path Compliance Eye Requirements for 16.0 GT/s with Ideal Adaptive TX Equalization

Parameter	Min	Max	Unit	Comments
V_{TXS}	19.0	1300	mV	Notes 1, 2, 4
V_{TXS_d}	19.0	1300		Notes 1, 2, 4
T_{TXS}	21.75		ps	Notes 1, 3, 4

Notes:

1. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the *PCI Express Base Specification*) is being transmitted during the test.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12} . The sample size for this measurement is required to be at least 2×10^6 UI.
3. T_{TXS} is the minimum eye width. The sample size for this measurement is required to be at least 2×10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXS} .
4. The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 5 dB of 85 Ω trace, at 8.0 GHz, followed by a non-root reference package behind a standard PCI Express edge-finger. This channel shall be referenced as the 16.0 GT/s System-Board Test Channel. The S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant Add-in Card.

4.8.17. System Board Transmitter Path Compliance Eye Diagram at 32.0 GT/s

The system board shall pass the eye diagram requirements with at least one of the TX equalization presets defined in the PCI Express Base Specification. The eye diagram requirements are evaluated after the behavioral CDR and the behavioral RX Equalization Algorithm defined in the PCI Express Base Specification are applied. The eye diagrams for the system boards's Transmitter path compliance at 32.0 GT/s are defined in Table 4-30.

Table 4-30. System Board Transmitter Path Compliance Eye Requirements for 32.0 GT/s with Ideal Adaptive TX Equalization

Parameter	Min	Max	Unit	Comments
V_{TXS}	17.5	1300	mV	Notes 1, 2, 4
T_{TXS}	9.688		ps	Notes 1, 3, 4

1. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the *PCI Express Base Specification*) is being transmitted during the test. The eye limits in this Table are different than *PCIe Express Base Specification* to account for Add-in Card crosstalk that is not present during measurement.
2. V_{TXS} is the minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12} . The sample size for this measurement is required to be at least 2×10^6 UI.
3. T_{TXS} is the minimum eye width. The recommended sample size for this measurement is at least 2×10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXS} .
4. The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 5.8 dB of 85 Ω trace, at 16.0 GHz, followed by a non-root reference package behind a standard PCI Express edge-finger. This channel shall be referenced as the 32.0 GT/s System-Board Test Channel. The S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant Add-in Card.

4.8.18. System Board Minimum Receiver Path Sensitivity Requirements at 2.5 GT/s

The minimum sensitivity values for the system board's Receiver path compliance at 2.5 GT/s are defined in Table 4-31. A representative eye diagram is shown in Figure 4-13.

Table 4-31: System Board Minimum Receiver Path Sensitivity Requirements for 2.5 GT/s

Parameter	Min	Max	Unit	Comments
V_{RXS}	445	1200	mV	Notes 1, 2, 5
V_{RXS_d}	312	1200	mV	Notes 1, 2, 5
T_{RXS}	287		ps	Notes 1, 3, 5
$T_{RXS-MEDIAN-to-MAX-JITTER}$	56.5		ps	Notes 1, 4, 5

Notes:

1. The system board reference clock is assumed for this specification. All Links are assumed active while generating this eye diagram. Compliance pattern is used when the receiver test is run.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{RXS_d}). V_{RXS} and V_{RXS_d} are differential peak-peak output voltages.
3. T_{RXS} is the eye width. The sample size for this measurement is 10^6 UI. This value can be reduced to 274 ps for simulation purpose at BER 10^{-12} .
4. $T_{RXS-MEDIAN-to-MAX-JITTER}$ is the maximum time delta between the jitter median and the maximum deviation from the median. The sample size for this measurement is 10^6 UI. This value can be increased to 63 ps for simulation purpose at BER 10^{-12} .
5. The values in this table are referenced to an ideal 100 Ω differential load at the end of 3-inch 85 Ω differential isolated traces behind a standard connector. The resultant values, when provided to the Receiver interconnect path of the system board, allow for a demonstration of compliance of the overall system board Receiver path. The sensitivity requirements are defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PCI Express Architecture PHY Test Specification*.

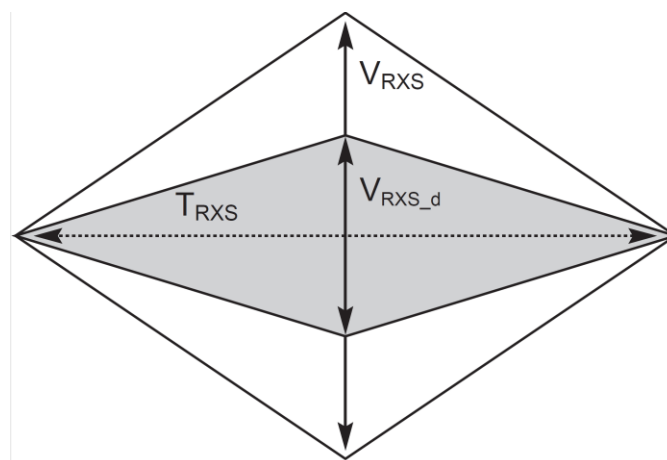


Figure 4-13. 2.5 GT/s and 5.0 GT/s Representative Composite Eye Diagram for System Board Receiver Path Compliance

4.8.19. System Board Minimum Receiver Path Sensitivity Requirements at 5.0 GT/s

The minimum sensitivity values for the system board's Receiver path compliance at 5.0 GT/s for a link that operates with 3.5 dB de-emphasis are defined in Table 4-32. For the system board's Receiver path compliance at 5.0 GT/s for a link that operates with 6.0 dB de-emphasis see Table 4-33.

Table 4-32: System Board Minimum Receiver Path Sensitivity Requirements for 5.0 GT/s at 3.5 dB De-emphasis

Parameter	Min	Max	Unit	Comments
V_{RXS}	380	1200	mV	Notes 1, 2, 3
V_{RXS_d}	380	1200	mV	Notes 1, 2, 3
1.5 – 100 MHz RMS Jitter	1.4		ps RMS	
< 1.5 MHz RMS Jitter	3.0		ps RMS	
1.5 – 100 MHz Dj	30		ps PP	
> 100 MHz Dj	27		ps PP	

Notes:

1. The system board reference clock is assumed for this specification. All Links are assumed active while generating this eye diagram. Modified compliance pattern is used when the receiver test is run.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{RXS_d}). V_{RXS} and V_{RXS_d} are differential peak-peak output voltages.
3. The values in this table are calibrated with a reference channel consisting of a 5.0 GT/s System Board Test Channel followed by a 5.0 GT/s Add-in Card Test Channel. After reference calibration, the 5.0 GT/s Add-in Card Test Channel is removed, and a standard PCI Express edge-finger is placed into the PCI Express connector to be tested. The resultant values, when provided to the Receiver interconnect path of the system board, allow for a demonstration of compliance of the overall system board Receiver path. The exact setup and methodology for injecting this signal into the Receiver interconnect path of the system board are not specified. The values in this table may need to be adjusted based on the exact test setup and methodology. For example, if the impedance of the test setup does not create the worst-case mismatch that could be present with a real Add-in Card or the test setup does not provide crosstalk (only a single Lane is tested, etc.), the values in this table must be adjusted accordingly.

Table 4-33: System Board Minimum Receiver Path Sensitivity Requirements for 5.0 GT/s at 6.0 dB De-emphasis

Parameter	Min	Max	Unit	Comments
V_{RXS}	306	1200	mV	Notes 1, 2, 3
V_{RXS_d}	260	1200	mV	Notes 1, 2, 3
1.5 – 100 MHz RMS Jitter	1.4		ps RMS	
< 1.5 MHz RMS Jitter	3.0		ps RMS	
1.5 – 100 MHz Dj	30		ps PP	
> 100 MHz Dj	27		ps PP	

Notes:

1. The system board reference clock is assumed for this specification. All Links are assumed active while generating this eye diagram. Modified compliance pattern is used when the receiver test is run.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{RXS_d}). V_{RXS} and V_{RXS_d} are differential peak-peak output voltages.
3. The values in this table are referenced to an ideal 100 Ω differential load behind 3 inches of isolated 85 Ω trace and a standard PCI Express connector. After reference calibration, the reference fixture is removed, and a standard PCI Express edge-finger is placed into the PCI Express connector to be tested. The resultant values, when provided to the Receiver interconnect path of the system board, allow for a demonstration of compliance of the overall system board Receiver path. The exact setup and methodology for injecting this signal into the Receiver interconnect path of the system board are not specified. The values in this table may need to be adjusted based on the exact test setup and methodology. For example, if the impedance of the test setup does not create the worst-case mismatch that could be present with a real Add-in Card or the test setup does not provide crosstalk (only a single Lane is tested, etc.), the values in this table must be adjusted accordingly.

4.8.20. System Board Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s

The minimum sensitivity values for the system board's Receiver path compliance at 8.0 GT/s are defined in Table 4-34. The receiver path shall be tested with a worst-case eye to verify that it achieves a $BER < 10^{-12}$. This worst-case eye is calibrated using TX equalization settings that are optimal with the reference equalizer for the calibration channel. After calibration, the test-generator's equalization settings may be adjusted using the transmitter equalization setting in the required TX equalization space preferred by the device under test, without changing any other parameter of the test signal or recalibrating the test signal.

If the test generator's TX equalization settings are adjusted away from the optimal settings and the test generator is not able to change transmitter equalization without impacting other calibrated parameters, then the other parameters must be adjusted back to the specified values.

If the test is not run in a way that produces the worst-case Crosstalk that would be present with all lanes active, the additional Crosstalk must be accounted for in some other way.

While the receiver's capacity to adapt its own equalization is part of the test described above, its ability to request the link partner's transmitter to change its equalization settings is tested by applying a signal whose equalization settings are sub-optimal compared to the jitter sensitivity test signal described above. For this signal, the reference receiver would not be able to achieve proper equalization by means of its own CTLE and DFE alone. Such a signal can be defined using the signal resulting from the calibration method described above and adjusting the test-generator equalization. If the RX under test is more capable than the reference (CTLE+DFE) receiver, the RX may not require the TX to change its equalization levels to achieve a $BER < 10^{-12}$. In any case, equalization settings resulting from this procedure shall be used for the above RX test and, if the RX requires the TX equalization to change, the change accommodates the test set-up used.

A specific methodology for this procedure is outside the scope of this specification.

Table 4-34: System Board Minimum Receiver Path Sensitivity Requirements for 8.0 GT/s

Parameter	Min	Max	Unit	Comments
V _{RX-EH-8G} Eye height	34	34	mV	Notes 1, 2, 4
T _{RX-EH-8G} Eye width	0.33	0.38	UI	Notes 1, 2
R _j (Random Jitter)	3		ps RMS	Notes 5, 6
S _j (Sinusoidal Jitter) 100 MHz	12.5		ps PP	Note 6
Differential Mode Sinusoidal Interference 2.1 GHz	14		mV PP	Note 3

Notes:

1. The system board reference clock is assumed for this specification. The 128/130b compliance pattern must be used during calibration for this test. Modified compliance pattern is used when the receiver test is run. Eye height and width values refer to $BER = 10^{-12}$.
2. The values in this table are initially calibrated with a reference channel consisting of an 8.0 GT/s system board Test Channel followed by 8.0 GT/s Add-in Card Test Channel at the TX SMP connectors on the Add-in Card Test Channel. The calibration is done with the same post processing as the Add-in Card 8.0 GT/s TX test. After reference calibration, the 8.0 GT/s Add-in Card Test Channel is removed, and the System Board Test Channel is connected to the System Board to be tested.
3. Eye height and width are specified after the application of the reference receiver. When the optimization of the reference receiver's CTLE and DFE yields an eye height and/or eye width larger than specified, the value for DM-interference is increased.
4. Eye height limits do not account for limitations in test equipment voltage resolution.
5. R_j is applied over the following range. The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz. While the nominal value is specified at 3.0 ps RMS, it may be adjusted to meet the value for T_{RX-EH-8G} Eye Width.
6. R_j and S_j are measured without post-processing filters.

4.8.21. System Board Minimum Receiver Path Sensitivity Requirements at 16.0 GT/s

The minimum sensitivity values for the system board's Receiver path compliance at 16.0 GT/s are defined in Table 4-35. The receiver path shall be tested with a worst-case eye to verify that it achieves a $BER < 10^{-12}$. This worst-case eye is calibrated using TX equalization settings that are optimal with the reference equalizer for the calibration channel. After calibration, the test-generator's equalization settings may be adjusted using the transmitter equalization setting in the required TX equalization space preferred by the device under test, without changing any other parameter of the test signal or recalibrating the test signal. This adjustment is done through running the PCI Express training protocol.

If the test generator's TX equalization settings are adjusted away from the optimal settings and the test generator is not able to change transmitter equalization without impacting other calibrated parameters – then the other parameters must be adjusted back to the calibrated values.

If the test is not run in a way that produces the worst-case Crosstalk that would be present with all lanes active, the additional Crosstalk must be accounted for in some other way.

Table 4-35: System Board Minimum Receiver Path Sensitivity Requirements for 16.0 GT/s

Parameter	Min	Max	Unit	Comments
V _{RX-EH-16G} Eye height	15	15	mV	Notes 1, 2, 4
T _{RX-EH-16G} Eye width	0.3	0.3	UI	Notes 1, 2
R _j (Random Jitter)	1.0		ps RMS	Notes 5, 6
S _j (Sinusoidal Jitter) 100 MHz	6.25		ps PP	Note 6
Differential Mode Sinusoidal Interference 2.1 GHz	14		mV PP	Note 3

Notes:

1. The system board reference clock is assumed for this specification. The 128/130b compliance pattern must be used during calibration for this test. Modified compliance pattern is used when the receiver test is run. Eye height and width values refer to BER = 10^{-12} .
2. The values in this table are initially calibrated with a reference channel consisting of a 16.0 GT/s System Board Test Channel followed by a 16.0 GT/s Add-in Card Test Channel. After reference calibration, the 16.0 GT/s Add-in Card Test Channel is removed, and the 16.0 GT/s System Board Test Channel is connected to the system board to be tested. The end to end CEM calibration channel must meet the requirements (insertion loss and return loss masks) defined for the 16.0 GT/s calibration channel in the *PCI Express Base Specification*.
3. Eye height and width are specified after the application of the reference receiver. V_{RX-EH-16G} and T_{RX-EH-16G} are adjusted following the same process described in the *PCI Express Base Specification* for calibrating the 16.0 GT/s stressed eye test. When the channel insertion loss is varied as part of the 16.0 GT/s stressed eye calibration process the variation must occur in the 16.0 GT/s System Board Test Channel portion of the channel.
4. Eye height limits do not account for limitations in test equipment voltage resolution.
5. R_j is applied over the following range. The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz.
6. R_j and S_j are measured without post-processing filters.

4.8.22. System Board Minimum Receiver Path Sensitivity Requirements at 32.0 GT/s

The minimum sensitivity values for the system board's Receiver path compliance at 32.0 GT/s are defined in Table 4-36. The receiver path shall be tested with a worst-case eye to verify that it achieves a BER < 10^{-12} . This worst-case eye is calibrated using TX equalization settings that are optimal with the reference equalizer for the calibration channel. After calibration, the test-generator's equalization settings may be adjusted using the transmitter equalization setting in the required TX equalization space preferred by the device under test, without changing any other parameter of the test signal or recalibrating the test signal. This adjustment is done through running the PCI Express training protocol.

If the test generator's TX equalization settings are adjusted away from the optimal settings and the test generator is not able to change transmitter equalization without impacting other calibrated parameters – then the other parameters must be adjusted back to the calibrated values.

If the test is not run in a way that produces the worst-case Crosstalk that would be present with all lanes active, the additional Crosstalk must be accounted for in some other way.

Table 4-36: System Board Minimum Receiver Path Sensitivity Requirements for 32.0 GT/s

Parameter	Nom	Unit	Comments
V _{RX-EH-32G} Eye height	15	mV	Notes 1, 2, 4, 7
T _{RX-EH-32G} Eye width	0.3	UI	Notes 1, 2, 7
R _j (Random Jitter)	0.5	ps RMS	Notes 5, 6, 7
S _j (Sinusoidal Jitter) 100 MHz	3.125	ps PP	Note 6, 7
Differential Mode Sinusoidal Interference 2.1 GHz	10	mV PP	Note 3, 7

Notes:

1. The system board reference clock is assumed for this specification. The 128/130b compliance pattern must be used during calibration for this test. Modified compliance pattern is used when the receiver test is run. Eye height and width values refer to BER = 10^{-12} .
2. The values in this table are initially calibrated with a reference channel consisting of a 32.0 GT/s System Board Test Channel followed by a 32.0 GT/s Add-in Card Test Channel. After reference calibration, the 32.0 GT/s Add-in Card Test Channel is removed, and the 32.0 GT/s System Board Test Channel is connected to the system board to be tested. The end to end CEM calibration channel must meet the requirements (insertion loss and return loss masks) defined for the 32.0 GT/s calibration channel in the *PCI Express Base Specification*.
3. Eye height and width are specified after the application of the reference receiver. V_{RX-EH-32G} and T_{RX-EH-32G} are adjusted following the same process described in the *PCI Express Base Specification* for calibrating the 32.0 GT/s stressed eye test. When the channel insertion loss is varied as part of the 32.0 GT/s stressed eye calibration process the variation must occur in the 32.0 GT/s System Board Test Channel portion of the channel.
4. Eye height limits do not account for limitations in test equipment voltage resolution.
5. R_j is applied over the following range. The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz.
6. R_j and S_j are measured without post-processing filters.
7. Refer to *PCI Express Architecture Phy Test Specification* for allowed tolerances around nominal values.

5. Add-in Card Auxiliary Power

A PCI Express CEM Add-in Card must adhere to the following power distribution, power-up, and power consumption requirements to ensure robust operation. Power may only be drawn from the following sources:

- The standard PCI Express edge connector as defined in Chapter 4.
- The dedicated Auxiliary Power Connector(s) defined in Chapters 7, 8, 9, and 10.

The power delivered from the PCI Express edge connector and the additional power delivered via the Auxiliary Power Connector(s) must be treated as coming from separate system power supply rails.

- The various sources of input power must not be electrically shorted at any point on a PCI Express Add-in Card.
 - This includes the power pins of separate Auxiliary Power Connectors if more than one Auxiliary Power Connector is present on the Add-in Card.
 - Within each auxiliary power connector, the power supplied to all pins must belong to the same power source. Those pins can be shorted together if desired.
 - Please note the +12V rail is present on the PCI Express edge connector and supported on some of the Auxiliary Power Connector(s). Separate sources of +12V must not be electrically shorted together.
- No specific power rail sequencing between the PCI Express edge connector and the Auxiliary Power Connector(s) can be assumed.
 - A PCI Express Add-in Card must handle all possible power sequence combinations.



IMPLEMENTATION NOTE

Labeling Considerations for Add-in Cards consuming more than 75W

Add-in Cards that require Auxiliary power Connectors are encouraged to follow the labeling described in the PCI Express Label Specification to help ensure the proper configuration of the Add-in Card.

5.1. Add-in Card Initial Power Level

The following power-up process permits a PCI Express Add-in Card to sense if the auxiliary connectors are plugged in and identify the initial power limits for each auxiliary connector.

The system power-up sequencing follows the Slot Power Limit Control mechanism as defined in the *PCI Express Base Specification*. The Add-in Card power-up sequencing is as follows:

At system power up, the permitted initial power from all power sources available to the Add-in Card depends on the combination of:

- The size of the PCI Express CEM Add-in Card edge-finger area.
- The number and type of Auxiliary Power Connector(s) installed on the card.

Note that each power source and connector is subject to, and limited to, the individual power ratings of the respective connectors.

Table 5-1 through Table 5-4 show the initial permitted power allowance from different auxiliary connectors.



Note: Note that all sources are additive. The total initial power to the Add-in Card is the Sum of the Initial Permitted Power values of each of the sources detected by the Add-in card.

For a sense pin to be detected, it must be connected to ground either directly in the power supply or via a jumper to an adjacent ground pin in the connector. It is recommended that for 12VHPWR and 48VHPWR connector, sense pin(s) be connected to ground in the power supply.

Table 5-1: PCI Express 2x3 Connector Initial Permitted Power

Sense Detected?	Initial Permitted Power from Connector at System Power Up
N	0 W available from 2x3 connector
Y	50 W available from 2x3 connector

Table 5-2: PCI Express 2x4 Connector Initial Permitted Power

Sense1 Detected?	Sense0 Detected?	Initial Permitted Power from Connector at System Power Up
N	N	0 W available from 2x4 connector
N	Y	50 W available from 2x4 connector
Y	N	Reserved condition, do not use.
Y	Y	100 W available from 2x4 connector

Table 5-3: PCI Express 12VHPWR Connector Initial Permitted Power

Sense0	Initial Permitted Power from Connector at System Power Up
Open	225 W available from connector (see Note 1 and 2)
Ground	375 W available from connector

Note:

1. The use of sideband sense lines is optional on the 12VHPWR connector. Use of Sense0 is required for power levels above minimum in this Table.
2. If the Add-in Card does not monitor these signals it must default to the lowest value in this table.

Table 5-4: PCI Express 48VHPWR Connector Initial Permitted Power

Sense1	Sense0	Initial Permitted Power from Connector at System Power Up
Open	Open	225 W available from connector (see Note 1 and 2)
Open	Ground	375 W available from connector
Ground	Open	Reserved condition, do not use. <ul style="list-style-type: none"> – Add-in Cards must treat this encoding as 375 W available from connector. – Systems must not supply this encoding. – Future revisions of this specification can alter this behavior
Ground	Ground	Reserved condition, do not use. <ul style="list-style-type: none"> – Add-in Cards must treat this encoding as 375 W available from connector. – Systems must not supply this encoding. – Future revisions of this specification can alter this behavior.

Note:

1. The use of sideband sense lines is optional on the 48VHPWR connector. Use of Sense0 and Sense1 is required for power levels above minimum in this Table.
2. If the Add-in Card does not monitor these signals it must default to the lowest value in this table.

If all the required power connections to the Add-in Card are not populated in such a way that results in the full initial power being available to the Add-in Card, then the card's operation is not guaranteed and is vendor implementation dependent.

5.2. Add-in Card Transition to Other Power Level

At system power-up the permitted initial power is dependent on Card edge-finger width and available Auxiliary Power connectors.

After Add-in Card reset is released and the PCI Express Link is up, the Add-in Card will receive the Set_Slot_Power_Limit message as defined in the *PCI Express Base Specification*. As referenced in those sections:

- If the Set_Slot_Power_Limit is smaller than the permitted initial power, the card can ignore the Set_Slot_Power_Limit message and continue to draw the same amount of power as initially permitted at system power up time.
- If the Set_Slot_Power_Limit is larger than or equal to the permitted initial power, the Add-in Card can then draw power up to the Set_Slot_Power_Limit in any order from the various power connectors connected to the card.
 - In relation to the Set_Slot_Power_Limit message, the permitted maximum power available to the Add-in Card depends on the combination of:
 - > The size of PCI Express CEM Add-in Card edge-finger area and
 - > The number and type of Auxiliary Power Connector(s) installed on the card.
- Intermediate values, not included in the discrete Slot Power Limit Values listed in the *PCI Express Base Specification*, are forbidden.

Note that each power source and connector is subject to, and limited to, the individual power ratings of the respective connectors.

Table 5-5 through Table 5-8 show the maximum permitted power from different auxiliary connectors.
 Note: All sources are additive.

- The total maximum power to the Add-in Card is the Sum of each of the maximum Permitted Power values of each of the sources detected by the Add-in Card.
- The total maximum power to the Add-in Card must never exceed the 600W limit

For a sense pin to be detected, it must be connected to ground either directly in the power supply or via a jumper to an adjacent ground pin in the connector. It is recommended that for 12VHPWR and 48VHPWR connector, sense pin(s) be connected to ground in the power supply.

Table 5-5: PCI Express 2x3 Connector Maximum Permitted Power

Sense Detected?	Maximum Power Permitted after Software Configuration
N	0 W available from 2x3 connector
Y	75 W available from 2x3 connector

Table 5-6: PCI Express 2x4 Connector Maximum Permitted Power

Sense1 Detected?	Sense0 Detected?	Maximum Power after Software Configuration
N	N	0 W available from 2x4 connector
N	Y	75 W available from 2x4 connector
Y	N	Reserved condition, do not use.
Y	Y	150 W available from 2x4 connector

Table 5-7: PCI Express 12VHPWR Connector Maximum Permitted Power

Sense0	Maximum Power after Software Configuration
Open	450 W (see Note 1 and 2)
Ground	600 W

Note:

1. The use of sideband sense lines is optional on the 12VHPWR connector. Use of Sense0 is required for power levels above minimum in this Table.
2. If the Add-in Card does not monitor these signals it must default to the lowest value in this Table.

Table 5-8: PCI Express 48VHPWR Connector Maximum Permitted Power

Sense1	Sense0	Maximum Power after Software Configuration
Open	Open	450 W (see Note 1 and 2)
Open	Ground	600 W
Ground	Open	Reserved condition, do not use. <ul style="list-style-type: none"> – CEM 5.0 Add-in Cards must treat this encoding as 600 W available from connector. – Systems must not supply this encoding. – Future revisions of this specification can alter this behavior
Ground	Ground	Reserved condition, do not use. <ul style="list-style-type: none"> – CEM 5.0 Add-in Cards must treat this encoding as 600 W available from connector. – Systems must not supply this encoding. – Future revisions of this specification can alter this behavior.

Note:

1. The use of sideband sense lines is optional on the 48VHPWR connector. Use of Sense1 and Sense0 is required for power levels above minimum in this Table.
2. If the Add-in Card does not monitor these signals it must default to the lowest value in this Table.

5.3. Optional Sideband Signal

With the introduction of the 12VHPWR and 48VHPWR Auxiliary Power connectors comes the addition of four optional sideband signals which can be used in conjunction with these High-Power Connectors.

The use of these optional sideband signals mapping to three features, as defined here, is not supported on the legacy 2x3 and 2x4 Auxiliary Power Connectors. Those legacy connectors are fully defined in Chapter 7 and Chapter 8.

The Add-in Card, high-power auxiliary cable, and power supply may optionally implement all, any, or none of the three features:

- SENSE1/SENSE0
- CARD_PWR_STABLE
- CARD_CBL_PRES#

See Figure 10-6 and Figure 10-7 for the physical location of the following optional sideband signals:

- **SENSE1/SENSE0:** These two optional sideband signals provide a mechanism for the Add-in Card to sense the Connector Initial Permitted Power and Connector Maximum Permitted Power limits for the cable and power supply. The initial power limit applies prior to the PCIe protocol stack being available and additional power being granted as defined in the *PCI Express Base Specification* (either Set_Slot_Power_Limit¹ or the Power Limit PM Sub State mechanism²). The maximum power limit is the maximum supported by this cable (regardless of additional power grants).

To ensure safety, the card designer is responsible for ensuring the power drawn from the cable never exceeds the limits indicated by SENSE1/SENSE0, even if erroneous messaging is given by Set_Slot_Power_Limit or Power Limit PM Sub State mechanism.

¹ The Set_Slot_Power_Limit mechanism is defined in the *PCI Express Base Specification*.

² The Power Limit PM Sub State mechanism is defined in the Combined Power ECN

For 48VHPWR connector, two SENSE signals have combined encoding for four unique power limits as listed in Table 5-4 and Table 5-8. For 12VHWPWR connector, only one sense pin (Sense0) is used and Pin#S4 is defined as No Connect.

If implemented, each of the SENSE signals from the auxiliary connector are connected on the Add-in Card to its own 4.7 k Ω pull-up resistor to the +3.3 V rail provided from the PCI Express CEM Add-in Card edge-finger. If the Add-in Card chooses to monitor the state of these SENSE signals it must do so using a high impedance 3.3 V logic compatible input device.

The power supply driving the high-power auxiliary cable, or the high-power auxiliary cable itself, must short the appropriate SENSE signals to ground or leave them open (high-impedance) to indicate the power limits associated with the power supply. These SENSE signals must not change state while the Add-in Card is operational.

If the SENSE signal is low (grounded), it is active. If the SENSE signal is open (high impedance), it is inactive.

If the cable or power supply does not implement the SENSE1 and SENSE0 signals, an Add-in Card that monitors these signals will detect both SENSE signals as inactive, and the Add-in Card must default to the lowest available power indicated in respective tables (see Table 5-3, Table 5-4, Table 5-7, and Table 5-8). Similarly, if Add-in Card does not monitor these signals the Add-in Card must default to the lowest available power indicated in respective tables. (see Table 5-3, Table 5-4, Table 5-7, and Table 5-8).

If the Add-in Card, attached cable, or power supply, chooses to support this sensing feature, then it must implement management of both SENSE signals.

If the Add-in Card implements the optional Power Budgeting Sense Detect register then the Add-in Card must monitor the SENSE signals.

Support for these optional sideband signals does not rely on any of the other optional sideband signals defined here and can be implemented independently of other optional sideband signals .

- **CARD_PWR_STABLE:** This optional sideband signal functions as a power-good indicator from the Add-in Card to the cable and power supply. Asserting this signal on the Add-in Card indicates its local power rails are within their operating limits. This signal can provide the power supply a fault detection from the Add-in Card and allows the power supply a protection opportunity.

If implemented, the CARD_PWR_STABLE signal is sourced on the Add-in Card in an open-collector/open-drain fashion. This signal is tied to a 100 k Ω pull-down resistor to ground on the Add-in Card.

If implemented, this signal traverses the optional sideband connector cable and is tied to a 4.7 k Ω pull-up resistor to +3.3V at the power supply. If the power supply or system monitors the state of the CARD_PWR_STABLE signal, it must do so with a high impedance 3.3 V logic compatible device input.

The Add-in Card sets this signal to open (high impedance) whenever its local power rails (critical to correct operations) are within their operating limits.

The Add-in Card logic actively drives this signal low whenever any of its local power rails (critical to correct operations) are outside of their operating limits. If a fault is detected, the Add-in Card must drive this signal for at least 100 ms, or until input power no longer meets the specifications of Section 4.1. If or when a fault is corrected the Add-in Card again sets this signal to open (high impedance).

Support for this optional sideband signal does not rely on any of the other optional sideband signals defined here and can be implemented independently of other optional sideband signals.

- **CARD_CBL_PRES#:** This optional sideband signal serves two functions:
 - Primary Function: It provides a signal from the Add-in Card to the power supply that the Add-in Card has detected the Auxiliary Power connector is correctly attached.
 - Secondary Function: It provides a signal from the power supply to the Add-in Card to be detected and presented to the Power Budgeting Sense Detect register³. This is for the purpose of allowing the system to correlate which system/power cable source is coupled to which connector on a specific PCIe card slot.

It is important to note this optional sideband signal is for the purpose of system power supply management support. It is not to be used by the Add-in Card to determine the power limits available to it. Those are handled solely using the SENSE0 and SENSE1 signals.

To support the primary function, the CARD_CBL_PRES# signal is tied to a 4.7 k Ω pull-down resistor to ground on the Add-in Card. If implemented, this signal traverses the optional sideband connector cable. If the power supply or system monitors the state of the CARD_CBL_PRES# signal, it must do so with a high impedance 3.3 V logic compatible device input. This signal must be low at the Add-in Card at all times when main power is absent. To detect the active low presence condition, the power supply or system may connect CARD_CBL_PRES# to a 100 k Ω pull-up resistor to +3.3 V (main or Vaux).

To support the secondary function, the Add-in Card reads this signal on a high impedance 3.3 V logic compatible input and records the logic high/low state in the Power Budgeting Sense Detect register³. The power supply is permitted to drive this signal high with a push-pull driver to 3.3 V (main or Vaux). The mechanism used to request that the power supply drive this signal high is outside the scope of this specification.

Card input logic should protect itself from errant system behavior of push-pull driving 3.3 V bias on CARD_CBL_PRES# when main power is off. Support for this optional sideband signal does not rely on any of the other optional sideband signals defined here and can be implemented independently of other optional sideband signals.

³ The Power Budgeting Sense Detect register is defined in the Combined Power ECN.

5.3.1. Optional Sideband Signal Parametric Specifications

5.3.1.1 DC Specifications

Table 5-9 lists the auxiliary signal DC specifications for optional sideband signals SENSE0, SENSE1, CARD_PWR_STABLE, and CARD_CBL_PRES#.

Table 5-9: Optional Sideband Signal DC Specifications – SENSE0, SENSE1, CARD_PWR_STABLE, and CARD_CBL_PRES#

Symbol	Parameter	Conditions	Min	Max	Unit
V _{HMAX}	Max High Voltage any pin			V _{cc3_3} + 0.5	V
V _{IL}	Input Low Voltage		-0.2	+0.8	V
V _{IH}	Input High Voltage		+2.0	V _{cc3_3} + 0.2	V
V _{OL}	Output Low Voltage	7.0 mA	-0.2	+0.5	V
V _{OH}	Output High Voltage (see note)	4.0 mA	+2.4	V _{cc3_3} + 0.2	V
R _{PULL-UP}	Pull-up / Pull-down Resistance tolerance		-10%	+10%	

Note: For Open-Collector/Open-Drain signal CARD_PWR_STABLE output a pull-up is required. There is no V_{OH} specification for this signal.

6. Card Connector Specification

The family of PCI Express vertical edge card connectors supports x1, x4, x8, and x16 Link widths to suit different bandwidth requirements. These connectors support the PCI Express signal and power requirements, as well as auxiliary signals used to facilitate the interface between the system board and Add-in Card hardware. This chapter defines the connector mating interfaces and footprints, as well as the electrical, mechanical, and environmental requirements.

6.1. Connector Pinout

Table 6-1 shows the pinout definition for the x1, x4, x8, and x16 PCI Express connectors. The auxiliary pins are identified in the shaded areas.

Table 6-1: PCI Express Connectors Pinout

Pin #	Name	Side B Description	Name	Side A Description
1	+12V	+12 V power	PRSNT1#	Presence detect
2	+12V	+12 V power	+12V	+12 V power
3	+12V	+12 V power	+12V	+12 V power
4	GND	Ground	GND	Ground
5	SMBCLK	SMBus (System Management Bus) clock	JTAG2	TCK (Test Clock), clock input for JTAG interface
6	SMBDAT	SMBus (System Management Bus) Data	JTAG3	TDI (Test Data Input)
7	GND	Ground	JTAG4	TDO (Test Data Output)
8	+3.3V	+3.3 V power	JTAG5	TMS (Test Mode Select)
9	JTAG1	TRST# (Test Reset), resets the JTAG interface	+3.3V	+3.3 V power
10	+3.3Vaux	+3.3 V auxiliary power	+3.3V	+3.3 V power
11	WAKE#	Signal for Link reactivation	PERST#	Fundamental reset
Mechanical Key				
12	CLKREQ#	Clock Request Signal	GND	Ground
13	GND	Ground	REFCLK+	Reference clock differential pair
14	PETp0	Transmitter differential pair, Lane 0	REFCLK-	
15	PETn0		GND	Ground
16	GND	Ground	PERp0	Receiver differential pair, Lane 0
17	PRSNT2#	Presence detect	PERn0	
18	GND	Ground	GND	Ground
End of the x1 Connector				
19	PETp1	Transmitter differential pair, Lane 1	MFG	Manufacturer Test Mode
20	PETn1		GND	Ground
21	GND	Ground	PERp1	Receiver differential pair, Lane 1
22	GND	Ground	PERn1	
23	PETp2	Transmitter differential pair, Lane 2	GND	Ground
24	PETn2		GND	Ground
25	GND	Ground	PERp2	Receiver differential pair, Lane 2

Pin #	Side B		Side A	
	Name	Description	Name	Description
26	GND	Ground	PERn2	
27	PETp3	Transmitter differential pair, Lane 3	GND	Ground
28	PETn3		GND	Ground
29	GND	Ground	PERp3	Receiver differential pair, Lane 3
30	PWRBRK#	Emergency Power Reduction	PERn3	
31	PRSNT2#	Presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved
End of the x4 connector				
33	PETp4	Transmitter differential pair, Lane 4	RSVD	Reserved
34	PETn4		GND	Ground
35	GND	Ground	PERp4	Receiver differential pair, Lane 4
36	GND	Ground	PERn4	
37	PETp5	Transmitter differential pair, Lane 5	GND	Ground
38	PETn5		GND	Ground
39	GND	Ground	PERp5	Receiver differential pair, Lane 5
40	GND	Ground	PERn5	
41	PETp6	Transmitter differential pair, Lane 6	GND	Ground
42	PETn6		GND	Ground
43	GND	Ground	PERp6	Receiver differential pair, Lane 6
44	GND	Ground	PERn6	
45	PETp7	Transmitter differential pair, Lane 7	GND	Ground
46	PETn7		GND	Ground
47	GND	Ground	PERp7	Receiver differential pair, Lane 7
48	PRSNT2#	Presence detect	PERn7	
49	GND	Ground	GND	Ground
End of the x8 Connector				
50	PETp8	Transmitter differential pair, Lane 8	RSVD	Reserved
51	PETn8		GND	Ground
52	GND	Ground	PERp8	Receiver differential pair, Lane 8
53	GND	Ground	PERn8	
54	PETp9	Transmitter differential pair, Lane 9	GND	Ground
55	PETn9		GND	Ground
56	GND	Ground	PERp9	Receiver differential pair, Lane 9
57	GND	Ground	PERn9	
58	PETp10	Transmitter differential pair, Lane 10	GND	Ground
59	PETn10		GND	Ground
60	GND	Ground	PERp10	Receiver differential pair, Lane 10
61	GND	Ground	PERn10	
62	PETp11	Transmitter differential pair, Lane 11	GND	Ground
63	PETn11		GND	Ground
64	GND	Ground	PERp11	Receiver differential pair, Lane 11
65	GND	Ground	PERn11	
66	PETp12	Transmitter differential pair, Lane 12	GND	Ground
67	PETn12		GND	Ground
68	GND	Ground	PERp12	Receiver differential pair, Lane 12
69	GND	Ground	PERn12	
70	PETp13	Transmitter differential pair, Lane 13	GND	Ground
71	PETn13		GND	Ground
72	GND	Ground	PERp13	Receiver differential pair, Lane 13
73	GND	Ground	PERn13	
74	PETp14	Transmitter differential pair, Lane 14	GND	Ground
75	PETn14		GND	Ground
76	GND	Ground	PERp14	Receiver differential pair, Lane 14
77	GND	Ground	PERn14	
78	PETp15	Transmitter differential pair, Lane 15	GND	Ground

Pin #	Side B		Side A	
	Name	Description	Name	Description
79	PETn15		GND	Ground
80	GND	Ground	PERp15	Receiver differential pair, Lane 15
81	PRSNT2#	Presence detect	PERn15	
82	RSVD	Reserved	GND	Ground
End of the x16 Connector				

Additional requirements:

- All Add-in Card edge-fingers must be present for pins A1/B1 through A82/B82. Depopulating connector pins and AIC edge-fingers is never allowed, except for a connector that supports a narrower link width than the mechanical length of the connector slot. For example, a x16 mechanical card edge with a x8 electrical width.
- The pins are numbered as shown in Figure 6-2 in ascending order from the left to the right, with side A on the top of the centerline and side B on the bottom of the centerline.
- The PCI Express interface pins PETpx, PETnx, PERpx, and PERnx are named with the following convention: “PE” stands for PCI Express, “T” for *Transmitter*, “R” for *Receiver*, “p” for *positive* (+), “n” for *negative* (-), and “x” is the Lane number.
- By default, PETpx and PETnx pins (the Transmitter differential pair of the connector) must be connected to the PCI Express Transmitter differential pair on the system board, and to the PCI Express Receiver differential pair on the Add-in Card.
- By default, PERpx and PERnx pins (the Receiver differential pair of the connector) shall be connected to the PCI Express Receiver differential pair on the system board, and to the PCI Express Transmitter differential pair on the Add-in Card.
- However, the “p” and “n” connections may be reversed to simplify PCB trace routing and minimize vias if needed. All PCI-Express Receivers incorporate automatic Lane Polarity Inversion as part of the Link Initialization and Training and will correct the polarity independently on each Lane. Refer to the *PCI Express Base Specification*.
- If the component on the system board or Add-in Card does not support the optional PCI Express Lane Reversal functions, they must connect each Transmitter and Receiver Lane to the Add-in Card connector lanes as shown in Table 6-1. For example, a x4 component must connect Lane 0 to 0, Lane 1 to 1, Lane 2 to 2, and Lane 3 to 3.
- If the component on the system board or Add-in Card supports the optional PCI Express Lane Reversal function, it may connect each Transmitter and Receiver Lane to the Add-in Card connector lanes as shown in Table 6-1 or it may connect the Transmitter and Receiver lanes using a reversed Lane ordering. Either Lane ordering may be used to simplify PCB trace routing and minimize vias. However, the transmitting and receiving lanes must connected with the same Lane ordering. For example, a x4 component may connect Lane 0 to 0, Lane 1 to 1, Lane 2 to 2, and Lane 3 to 3 or it may connect Lane 0 to 3, Lane 1 to 2, Lane 2 to 1, and Lane 3 to 0.
- The connectors and the Add-in Cards are keyed such that smaller Add-in Cards can be put in larger connectors. For example, a x1 card can be inserted into the x4, x8, and x16 connectors. This is referred to as up-plugging.
- Support for down-plugging is outside the scope of this specification.
- Two ground pins separate adjacent differential pairs to manage the connector crosstalk.
- See Chapter 2 for auxiliary signals description and implementation, except the +3.3Vaux and PRSNT1# and PRSNT2# pins. The requirements for +3.3Vaux are discussed in Chapter 4 and presence detect is discussed in Chapter 3.

- PRSNT1# and PRSNT2# pins are for card presence detect. Additional PRSNT2# pins in the x4, x8, and x16 PCI Express connectors are for supporting up-plugging. See Chapter 3 for detailed discussions on presence detect.
- Power pins (+3.3V, +3.3Vaux, and +12V) are defined based on the PCI Express power delivery requirements specified in Chapter 4, with the connector contact carrying capability being 1.1 A per pin. The power that goes through the connector shall not exceed the maximum power specified for a given Add-in Card size, as defined in Section 4.2.
- If an optional pin function is not implemented, that pin must not be used for any other purpose. Unless otherwise specified (see Section 11.2.5), reserved pins (RSVD) must not be connected on either the Add-in Card or system board side of the connector. These pins are reserved for use with future versions of this specification. Non-standard use of these pins may result in interoperability issues.

6.2. Connector Interface Definitions

The PCI Express through-hole connector outline and footprint are shown in Figure 6-1 and Figure 6-2. For clarity, sentry vias, which are ground placed adjacent to auxiliary and Reserved signal pins, are not depicted in Figure 6-2. Sentry via requirements are detailed in Section 11.3.1. The surface mount connector outline and footprint are shown in Figure 6-3 and Figure 6-4. The Add-in Card edge-finger dimensions are shown in Figure 6-5. The Add-in Card edge-finger dimensions are independent of the connector mounting style.



IMPLEMENTATION NOTE

Through-hole connectors with appropriate optimization are supported for speeds up to 16GT/s. For 32GT/s, only surface mount connectors must be used.

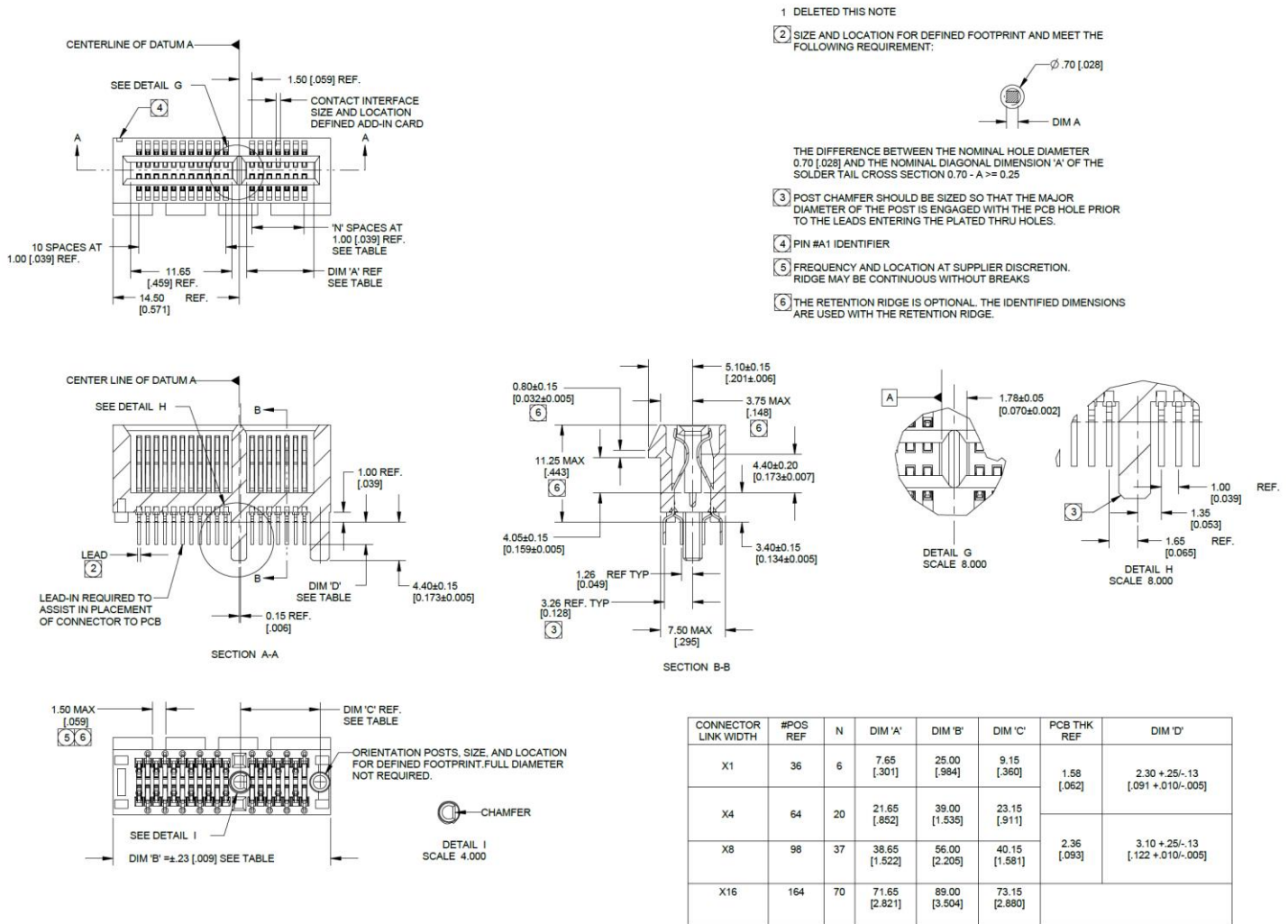
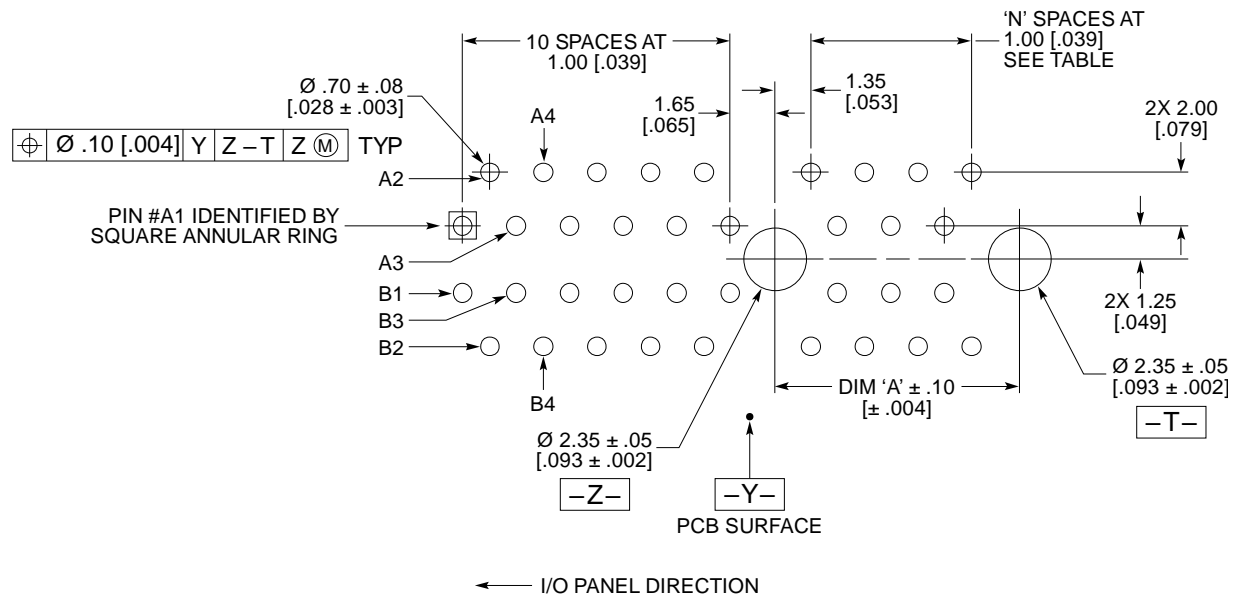


Figure 6-1: Through-Hole Mount Connector Outline



CONNECTOR LINK WIDTH	# POS REF	N	DIM 'A'
X1	36	6	9.15 [.360]
X4	64	20	23.15 [.911]
X8	98	37	40.15 [1.581]
X16	164	70	73.15 [2.880]

A-0900

Note: Sentry vias are not shown.

Figure 6-2: Through-Hole Mount Connector Footprint

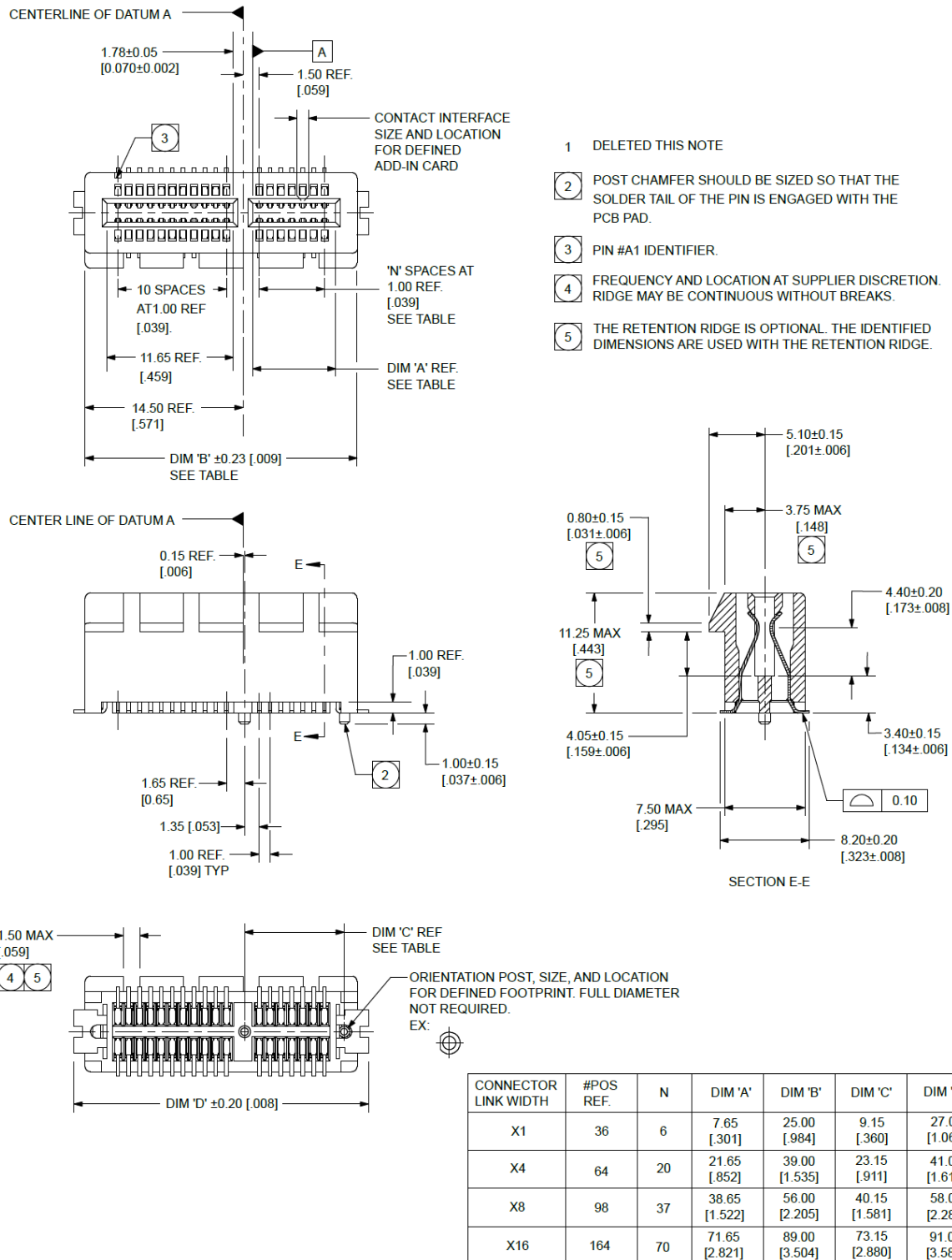
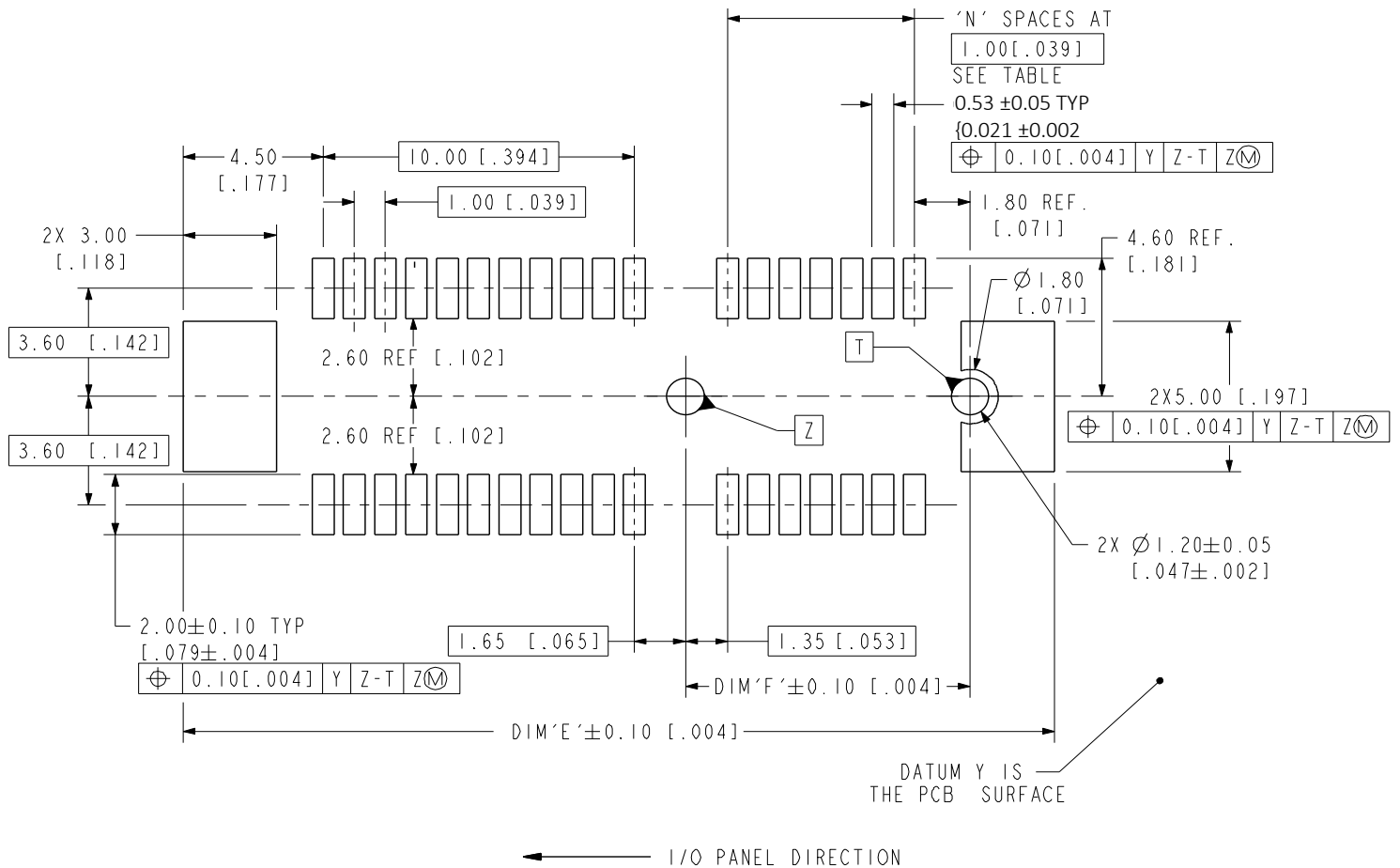


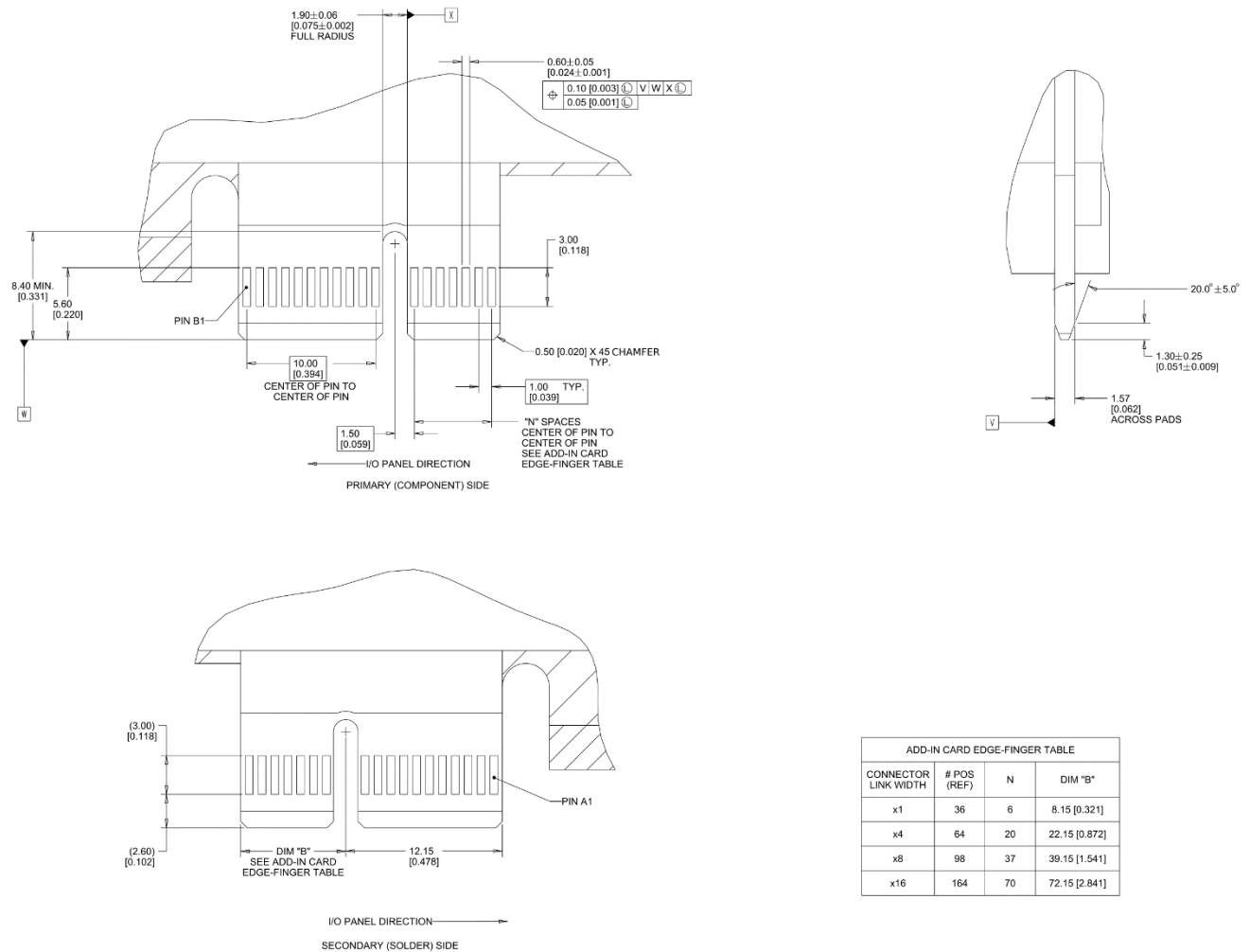
Figure 6-3: Surface Mount Connector Outline



CONNECTOR LINK WIDTH	#POS REF.	N	DIM'E'	DIM'F'
X1	36	6	28.00 [1.102]	9.15 [.360]
X4	64	20	42.00 [1.654]	23.15 [.911]
X8	98	37	59.00 [2.323]	40.15 [1.581]
X16	164	70	92.00 [3.622]	73.15 [2.880]

NOTE: TOLERANCE UNLESS OTHER NOTED IS ± 0.13 [0.005].

Figure 6-4: Surface Mount Connector Footprint



1. TOLERANCE UNLESS OTHERWISE NOTED: ± 0.13 [0.005].
2. SEE Figure 11-22 FOR KEEPOUT AREAS IN THE GOLD FINGER REGION.

Figure 6-5: Add-in Card Edge-Finger Dimensions

Be aware of the following points:

- The connector has a 1.00 mm contact pitch.
- The contact shall be pre-loaded.
- The system PCB through-hole mount connector footprint (Figure 6-2) requires two 2.35 mm diameter location holes, accepting either plastic or metal pegs/posts or metal board locks. The two 2.35 mm diameter location holes may either be drilled or plated through-holes (PTH). Plated through-holes enable the soldering of a connector with metal guideposts to provide more secure retention for larger/heavier Add-in Cards. Metal board locks are also allowed, although Figure 6-1 shows only the plastic pegs on the connector housing.

- The surface mount technology connector footprint (Figure 6-4) requires two 1.20 mm holes, working with either plastic or metal pegs / posts or metal board locks. The two 1.20 mm diameter location holes may either be drilled or plated through-holes.
- Figure 6-5 defines only the mating interface related dimensions. Other Add-in Card dimensions are defined in Chapter 11.
- The PRSNT1# and PRSNT2# edge-fingers shown in Figure 6-5 are 3.0 mm long, the same length as the other fingers. Those pins are designated as A1, B17, B31, B48, and B81, where applicable. This is a change from CEM 4.0.
- As shown in Figure 6-1 and Figure 6-3, an optional ridge feature is defined on the top of the connector housing on one side. This feature can be used to facilitate card retention. A retention clip may be mounted on an Add-in Card and latched on the ridge.
- Two types of Add-in Cards must be “retention ready”:
 - Cards that, in the judgment of the card manufacturer, have sufficient weight or length that the card may need an additional retention point for stability.
 - Retention ready means that the Add-in Card manufacturer must have selected (or created) a retention mechanism and made provisions on the card to facilitate the retention mechanism.
 - The full-length card, 321.00 mm (12.283 inches) long, is considered retention ready. The mounting holes on one end of the full-length card allow the optional PCI card retainer to be installed to secure the card (see Section 11.1).
- Detailed connector contacts and housing designs are up to each connector vendor, as long as the requirements of form, fit, and function are met.
- Straddle mount connectors (i.e., connectors that straddle the edge of a circuit board with one set of connections, with the “A” side, connected to pads on the top of the board and the other set of connections “B” side connected to the bottom of the board) may require additional design considerations to support retention of the Add-in Card and are not explicitly covered in this specification.

6.3. Signal Integrity Requirements and Test Procedures

6.3.1. Signal Integrity Requirements

The following procedure documents (outlined in the ANSI Electronics Industry Alliance (EIA) Standards) shall be followed:

- EIA 364-101 – Attenuation Test Procedure for Electrical Connectors, Sockets, Cable Assemblies, or Interconnection Systems
- EIA 364-90 – Crosstalk Ratio Test Procedure for Electrical Connectors, Sockets, Cable Assemblies, or Interconnection Systems
- EIA 364-108 – Impedance, Reflection Coefficient, Return Loss, and VSWR Measured in the Time and Frequency Domain Test Procedure for Electrical Connectors, Sockets, Cable Assemblies, or Interconnection Systems

6.3.2. Signal Integrity Requirements and Test Procedures for 2.5 GT/s Support

A common electrical test fixture is specified and used for evaluating connector signal integrity. The test fixture will have 0.1524 mm (6.0 mil) wide 50 Ω single-ended traces that must be uncoupled. The impedance variation of those traces shall be controlled within $\pm 5\%$. Refer to the *PCI Express Connector High Speed Electrical Test Procedure* for detailed discussions on the test fixture.

Detailed testing procedures are specified in the *PCI Express Connector High Speed Electrical Test Procedure*. This document must be used in conjunction with the standard test fixture.

For the insertion loss and return loss tests, the measurement shall include 1.2-inch-long PCB traces (0.6 inches on the system board and 0.6 inches on the Add-in Card). The edge-finger pad is not counted as Add-in Card PCB trace; it is considered part of the connector interface. The 1.2-inch PCB trace included in the connector measurement is a part of the trace length allowed on the system board. See Section 4.7 for a discussion of the electrical budget.

Either single-ended measurements that are processed to extract the differential characteristics or true differential measurements are allowed. The detailed definition and description of the test fixture and the measurement procedures are provided in the *PCI Express Connector High Speed Electrical Test Procedure*.

An additional consideration for the connector electrical performance is the connector-to-system board and the connector to Add-in Card launches. The connector through-hole pad and antipad sizes shall follow good electrical design practices to minimize impedance discontinuity. On the Add-in Card, the ground and power planes underneath the PCI Express high-speed signals (edge-fingers) shall be removed. Otherwise, the edge-fingers will have too much capacitance and greatly degrade connector performance. A more detailed discussion on the Add-in Card electrical design can be found in the *PCI Express Connector High Speed Electrical Test Procedure*.

Table 6-2 lists the electrical signal integrity parameters, requirements, and test procedures.

Table 6-2: Signal Integrity Requirements and Test Procedures for 2.5 GT/s Support

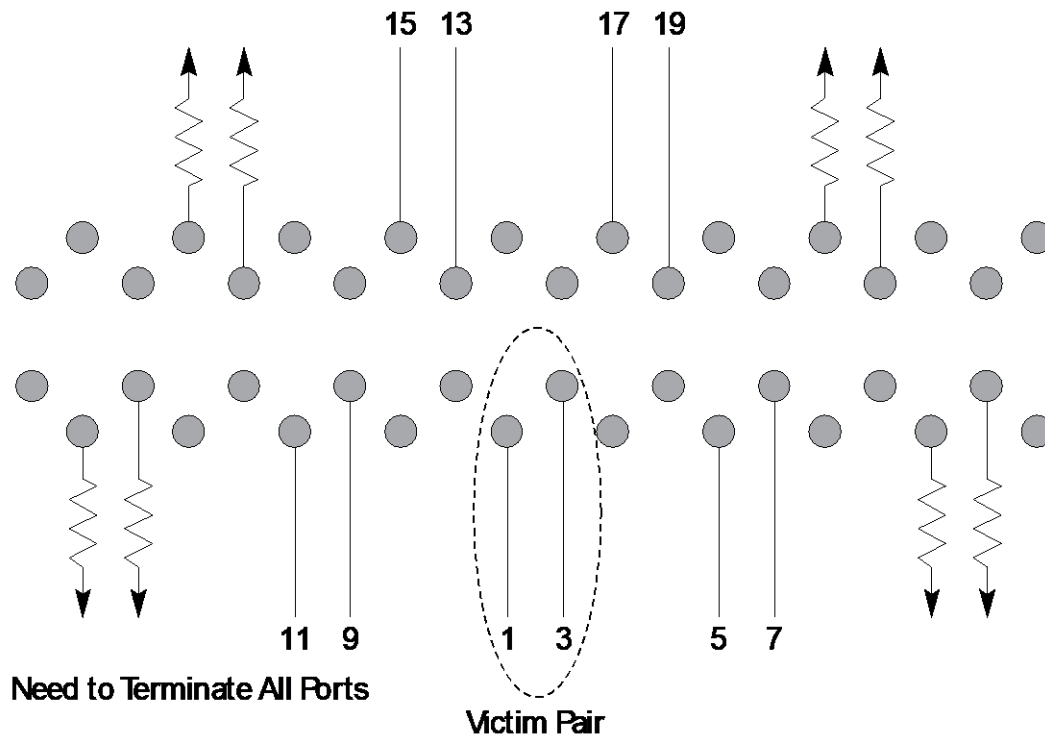
Parameter	Procedure	Requirements
Differential Insertion Loss (DDIL)	<p>EIA 364-101</p> <p>The EIA standard must be used with the following considerations:</p> <ol style="list-style-type: none"> 1. The step-by-step measurement procedure is outlined in the <i>PCI Express Connector High Speed Electrical Test Procedure</i> (see Note 1 below). 2. A common test fixture for connector characterization shall be used. 3. This is a differential insertion loss requirement. Either true differential measurements must be made or post processing of the single-ended measurements must be done to extract the differential characteristics of the connector. The methodology of doing so is covered in the <i>PCI Express Connector High Speed Electrical Test Procedure</i> (Note 1). 	<p>≥ -1 dB for $f \leq 1.25$ GHz;</p> <p>$\geq -[1.6*(f - 1.25) + 1]$ dB for $1.25 \text{ GHz} < f \leq 3.75 \text{ GHz}$</p> <p>(for example, ≥ -5 dB at $f = 3.75 \text{ GHz}$)</p>

Parameter	Procedure	Requirements
Differential Return Loss (DDRL)	<p>EIA 364-108</p> <p>The EIA standard must be used with the following considerations:</p> <ol style="list-style-type: none"> 1. The step-by-step measurement procedure is outlined in the <i>PCI Express Connector High Speed Electrical Test Procedure</i> (Note 1). 2. A common test fixture for connector characterization shall be used. 3. This is a differential return loss requirement. Either true differential measurements must be made or post processing of the single-ended measurements must be done to extract the differential characteristics of the connector. The methodology of doing so is covered in the <i>PCI Express Connector High Speed Electrical Test Procedure</i> (Note 1). 	≤ -12 dB for $f \leq 1.3$ GHz; ≤ -7 dB for $1.3 \text{ GHz} < f \leq 2$ GHz; ≤ -4 dB for $2 \text{ GHz} \leq 3.75$ GHz
Intra-pair Skew	Intra-pair skew must be achieved by design; measurement not required.	5 ps max
Differential Near End Crosstalk: DDNEXT	<p>EIA 364-90</p> <p>The EIA standard must be used with the following considerations:</p> <ol style="list-style-type: none"> 1. The crosstalk requirement is with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector, as illustrated in Figure 6-6. This is reflected in the measurement procedure. 2. The step-by-step measurement procedure is outlined in the <i>PCI Express Connector High Speed Electrical Test Procedure</i>. 3. A common test fixture for connector characterization shall be used. 4. This is a differential crosstalk requirement between a victim differential signal pair and all its adjacent differential signal pairs. Either true differential measurements must be made, or post processing of the single-ended measurements must be done to extract the differential crosstalk of the connector. The methodology of doing so is covered in the <i>PCI Express Connector High Speed Electrical Test Procedure</i> (see Note 1). 	≤ -32 dB for $f \leq 1.25$ GHz; $\leq -[32 - 2.4 * (f - 1.25)]$ dB for $1.25 \text{ GHz} < f \leq 3.75$ GHz (for example, ≤ -26 dB at $f = 3.75$ GHz)

Notes:

1. The *PCI Express Connector High Speed Electrical Test Procedure* is available separately.
2. A typical approach to making these measurements is with a network analyzer or a TDR oscilloscope. Differential measurements require the use of a two port (or a four port) instrument to measure the connector. The differential parameters may be measured directly if the equipment supports "True" differential excitation ("True" differential excitation is the simultaneous application of a signal to one line of the pair and a 180-degree phase shifted version of the signal to the second line of the pair). If single-ended measurements are made, the differential connector parameters must be derived from the single-ended measurements as defined in the *PCI Express Connector High Speed Electrical Test Procedure*.
3. The connector shall be targeted for a 100 Ω differential impedance.

In Figure 6-6, pairs marked as 11-9, 5-7, 15-13, and 17-19 are the adjacent pairs with respect to the victim pair 1-3.



CM14761

Figure 6-6: Illustration of Adjacent Pairs

6.3.3. Signal Integrity Requirements and Test Procedures for 5.0 GT/s Support

An electrical test fixture must be used for evaluating connector signal integrity. The test fixture effects, not including the connector via, are de-embedded from measurements. Test fixture requirements and recommendations are provided in Section 6.3.3.1.

Table 6-3 lists the electrical signal integrity parameters, requirements, and test procedures.

Table 6-3: Signal Integrity Requirements and Test Procedures for 5.0 GT/s Support

Parameter	Procedure	Requirements
Differential Insertion Loss (DDIL)	EIA 364-101 The EIA standard shall be used with the following considerations: 1. The measured differential S-parameter shall be referenced to an 85 Ω differential impedance. 2. The test fixture shall meet the test fixture requirement defined in Section 6.3.3.1. 3. The test fixture effect shall be removed from the measured S-parameters. See Note 1.	≥ -0.5 dB for $f \leq 2.5$ GHz; $\geq -[0.8*(f - 2.5)+0.5]$ dB for $2.5 \text{ GHz} < f \leq 5 \text{ GHz}$ (for example, ≥ -2.5 dB at $f = 5 \text{ GHz}$); $\geq -[3.0*(f - 5)+2.5]$ dB for $5 \text{ GHz} < f \leq 7.5 \text{ GHz}$ (for example, ≥ -10 dB at $f = 7.5 \text{ GHz}$)
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard shall be used with the following considerations: 1. The measured differential S-parameter shall be referenced to an 85 Ω differential impedance. 2. The test fixture shall meet the test fixture requirement given in Section 6.3.3.1. 3. The test fixture effect shall be removed. See Note 1.	≤ -15 dB for $f \leq 3 \text{ GHz}$; ≤ -5 dB for $3 \text{ GHz} < f \leq 5 \text{ GHz}$; ≤ -1 dB for $5 \text{ GHz} < f \leq 7.5 \text{ GHz}$
Intra-pair Skew	Intra-pair skew is achieved by design; measurement not required.	5 ps max
Differential Near End Crosstalk (DDNEXT)	EIA 364-90 The EIA standard must be used with the following considerations: 1. The crosstalk requirement is with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector, as shown in Figure 6-11. 2. This is a differential crosstalk requirement between a victim differential signal pair and all its adjacent differential signal pairs. The measured differential S-parameter shall be referenced to an 85 Ω differential impedance.	≤ -32 dB up to 2.5 GHz; ≤ -26 dB for $2.5 \text{ GHz} < f \leq 5 \text{ GHz}$; ≤ -20 dB for $5 \text{ GHz} < f \leq 7.5 \text{ GHz}$

Notes:

1. The specified S-parameter requirements are for connector only, not including the test fixture effect.
2x Thru de-embedding, TRL and other methods for calibration and fixture removal are allowed.

6.3.3.1 Test Fixture Requirements

The test fixture for connector S-parameter measurement must be designed and built to the following requirements:

- The test fixture shall be an FR-4 based PCB of the microstrip structure; the dielectric thickness or stackup shall be approximately 0.102 mm (4 mil).
- The total thickness of the test fixture PCB shall be 1.57 mm (62 mil) and the test Add-in Card must be a break-out card fabricated in the same PCB panel for the fixture.
- The measurement signals shall be launched into the connector from the top of the test fixture, capturing the through-hole stub effect.
- Traces between the connector and measurement ports (SMA or microprobe) must be uncoupled.
- The trace lengths between the connector and measurement port shall be minimized. The maximum trace length shall not exceed 45.72 mm (1800 mil). The trace lengths between the connector and measurement port on the test baseboard and Add-in Card must be equal. The edge-finger pad is not counted as Add-in Card PCB trace; it is considered part of the connector interface.
- All the traces on the test baseboard and Add-in Card must be held to a characteristic impedance of 50 Ω with a tolerance of $\pm 7\%$.
- The test Add-in Card edge-finger pads shall be fabricated per mechanical specification defined in Figure 6-5. The ground plane immediately underneath the edge-finger pads must be removed.
- The through-hole on the test baseboard shall have the following stackup: 0.711 mm (28 mil) finished hole, 1.067 mm (42 mil) pad, and 1.473 mm (58 mil) antipad.
- Use of SMA connectors is recommended. The SMA launch structure shall be designed to minimize the connection discontinuity from SMA to the trace. The impedance range of the SMA seen from a TDR with a 60 ps rise time is recommended to be within 50 ± 7 Ω .
- If a fixture with other characteristics is used, the fixture effects must be reliably removed and must not impact measurement accuracy.

6.3.4. Signal Integrity Requirements and Test Procedures for 8.0 GT/s Support

An electrical test fixture must be used for evaluating connector signal integrity. The test fixture effects, not including the connector via, are de-embedded from measurements. Test fixture requirements and recommendations are provided in Section 6.3.4.1.

Table 6-4 lists the electrical signal integrity parameters, requirements, and test procedures.

Table 6-4: Signal Integrity Requirements and Test Procedures for 8.0 GT/s Support

Parameter	Procedure	Requirements
Differential Insertion Loss (DDIL)	EIA 364-101 The EIA standard shall be used with the following considerations: 1. The measured differential S-parameter shall be referenced to an 85 Ω differential impedance. 2. The test fixture shall meet the test fixture requirement defined in Section 6.3.4.1. 3. The test fixture effect shall be removed from the measured S-parameters. See Note 1.	≥ -0.5 dB up to 2.5 GHz; $\geq -[0.8*(f - 2.5)+0.5]$ dB for $2.5 \text{ GHz} < f \leq 5 \text{ GHz}$ (for example, ≥ -2.5 dB at $f = 5 \text{ GHz}$); $\geq -[3.0*(f - 5)+2.5]$ dB for $5 \text{ GHz} < f \leq 12 \text{ GHz}$ (for example, ≥ -10 dB at $f = 7.5 \text{ GHz}$)
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard shall be used with the following considerations: 1. The measured differential S-parameter shall be referenced to an 85 Ω differential impedance. 2. The test fixture shall meet the test fixture requirement in Section 6.3.4.1. 3. The test fixture effect shall be removed. See Note 1.	≤ -15 dB up to 3 GHz; $\leq 5*f - 30$ dB for $3 \text{ GHz} < f \leq 5 \text{ GHz}$; ≤ -1 dB for $5 \text{ GHz} < f \leq 12 \text{ GHz}$
Intra-pair Skew	Design must achieve intra-pair skew; measurement not required.	5 ps max
Differential Near End Crosstalk (DDNEXT)	EIA 364-90 The EIA standard must be used with the following considerations: 1. The crosstalk requirement is with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector, as illustrated in Figure 6-6. 2. This is a differential crosstalk requirement between a victim differential signal pair and all of its adjacent differential signal pairs. The measured differential S-parameter shall be referenced to an 85 Ω <i>differential</i> impedance.	≤ -32 dB up to 2.5 GHz; ≤ -26 dB for $2.5 \text{ GHz} < f \leq 5 \text{ GHz}$; ≤ -20 dB for $5 \text{ GHz} < f \leq 10 \text{ GHz}$; < -10 dB for $10 \text{ GHz} < f \leq 12 \text{ GHz}$

Notes:

1. The specified S-parameter requirements are for connector only, not including the test fixture effect. 2x Thru de-embedding, TRL and other methods for calibration and fixture removal are allowed.

6.3.4.1 Test Fixture Requirements

The test fixture for connector S-parameter measurement must be designed and built to the following requirements:

- The test fixture shall be an FR-4 based PCB of the microstrip structure; the dielectric thickness or stackup shall be approximately 0.102 mm (4 mil).
- The total thickness of the test fixture PCB shall be 1.57 mm (62 mil) and the test Add-in Card must be a break-out card fabricated in the same PCB panel for the fixture.
- The measurement signals shall be launched into the connector from the top of the test fixture, capturing the through-hole stub effect.
- Traces between the connector and measurement ports (SMA or microprobe) must be uncoupled.

- The trace lengths between the connector and measurement port shall be minimized. The maximum trace length shall not exceed 46 mm (1800 mil). The trace lengths between the connector and measurement port on the test baseboard and Add-in Card must be equal. The edge-finger pad is not counted as Add-in Card PCB trace; it is considered part of the connector interface.
- All traces on the test baseboard and Add-in Card must be held to a characteristic impedance of 50 Ω with a tolerance of $\pm 7\%$.
- The test Add-in Card edge-finger pads shall be fabricated per mechanical specification defined in Figure 6-5. The ground plane immediately underneath the edge-finger pads must be removed.
- The through-hole on the test baseboard shall have the following stackup: 0.711 mm (28 mil) finished hole, 1.067 mm (42 mil) pad, and 1.473 mm (58 mil) antipad.
- Use of SMA connectors is recommended. The SMA launch structure shall be designed to minimize the connection discontinuity from SMA to the trace. The impedance range of the SMA seen from a TDR with a 30 ps rise time is recommended to be within $50 \pm 7 \Omega$.
- If a fixture with other characteristics is used, the fixture effects must be reliably removed and must not impact measurement accuracy.

6.3.5. Signal Integrity Requirements and Test Procedures for 16.0 GT/s Support

An electrical test fixture must be used for evaluating connector signal integrity. The test fixture effects are de-embedded from measurements. Test fixture requirements and recommendations are provided.

Table 6-5 lists the electrical signal integrity parameters, requirements, and test procedures.

Table 6-5: Signal Integrity Requirements and Test Procedures for 16.0 GT/s Support

Parameter	Procedure	Requirements
Differential Insertion Loss (DDIL)	EIA 364-101 The EIA standard shall be used with the following considerations: 1. The measured differential S-parameter shall be referenced to an 85 Ω differential impedance. 2. The test fixture shall meet the test fixture requirement defined in Section 6.3.5.1. 3. The test fixture effect shall be removed from the measured S-parameters. See Note 1.	≥ -0.5 dB for $f \leq 4$ GHz; $\geq [-0.25 * f + 0.5]$ dB for $4 \text{ GHz} < f < 8 \text{ GHz}$ (for example -1.5 dB at 8 GHz); $\geq [-0.75 * f + 4.5]$ dB for $8 \text{ GHz} < f < 10 \text{ GHz}$ (for example: -3.0 dB at 10 GHz)
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard shall be used with the following considerations: 1. The measured differential S-parameter shall be referenced to an 85 Ω differential impedance. 2. The test fixture shall meet the test fixture requirement in Section 6.3.5.1. 3. The test fixture effect shall be removed. See Note 1.	≤ -15 dB up to 3 GHz; $\leq [5 * f - 30]$ dB for $3 < f < 4.4 \text{ GHz}$; (for example: -10 dB at 4 GHz); ≤ -8 dB from 4.4 to 10 GHz
Intra-pair Skew	Intra-pair skew must be achieved by design; measurement not required.	5 ps max

Parameter	Procedure	Requirements
Differential Near End Crosstalk (DDNEXT)	EIA 364-90 The EIA standard must be used with the following considerations: 1. The crosstalk requirement is with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector, as listed in Table 6-6. 2. This is a differential crosstalk requirement between a victim differential signal pair and all its adjacent differential signal pairs. The measured differential S-parameter shall be referenced to an 85 Ω differential impedance.	≤ -32 dB up to 8 GHz and -20 dB from 8 GHz to 10 GHz

Notes:

- The specified S-parameter requirements are for connector only, not including the test fixture effect. 2x Thru de-embedding, TRL and other methods for calibration and fixture removal are allowed.

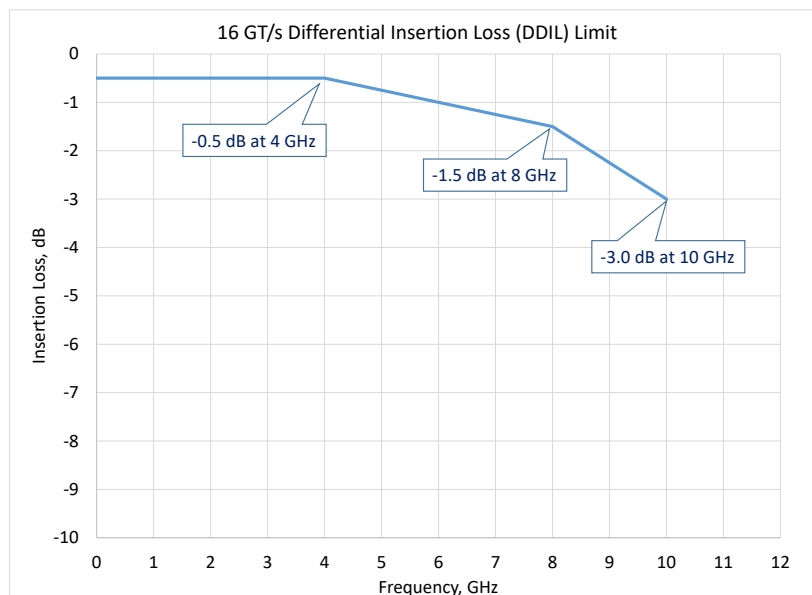


Figure 6-7. Differential Insertion Loss Limits for 16.0 GT/s Operation

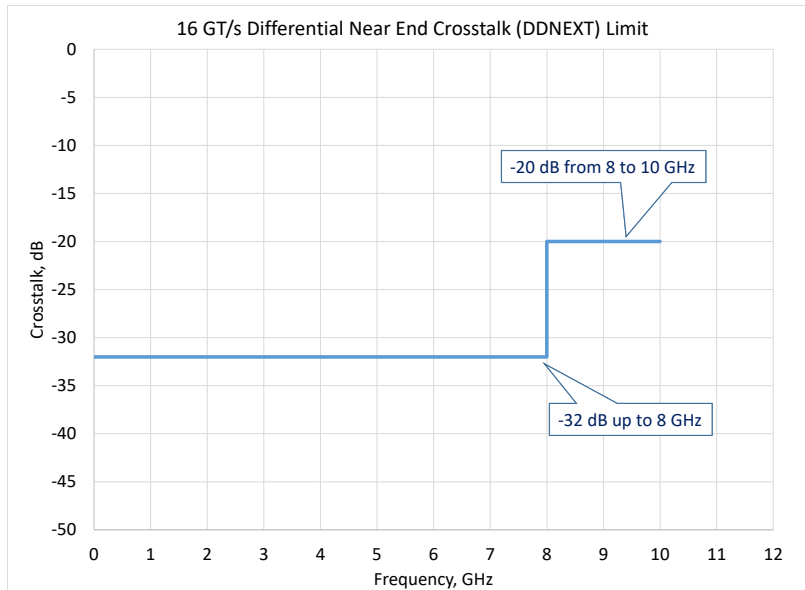


Figure 6-8. Differential Near End Crosstalk Limits for 16.0 GT/s operation

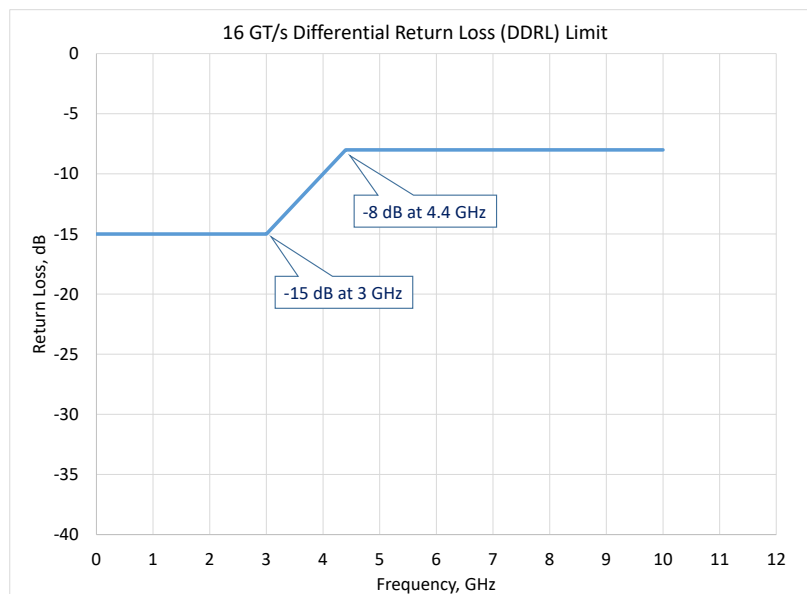


Figure 6-9. Differential Return Loss Limits for 16.0 GT/s operation

6.3.5.1 Test Fixture Requirements

A test fixture for connector S-parameter measurement must be designed and built to the following:

- The test fixture used for measuring S-parameter will comprise a baseboard and mating Add-in Card fabricated from the same PCB panel. The total thickness of the boards measured across the Add-in Card edge-fingers, must be 1.57 mm (62 mil).

- The PCB test fixture must be an FR-4 based material, or of a lower loss material with a relative permittivity of 3.6 or greater. Dielectric loss factor is not specified.
- The test PCB must have a microstrip structure; the microstrip's dielectric thickness or stackup are recommended to be approximately 0.102 mm (4 mil).
- The interconnect traces on all boards must be routed uncoupled (single-ended) where possible. Some method of mitigating fiber weave effects must be applied. This can include off-axis routing or board rotation on the PCB panel.
- The trace lengths between the connector and measurement port must be minimized. The maximum trace length must not exceed 48 mm (1.9 inches). The trace lengths between the connector and measurement port on the test baseboard and Add-in Card must be equal within 0.5 mil. The edge-finger pad is not counted as Add-in Card PCB trace; it is considered part of the connector interface.
- Separate PCB structures must be included to support de-embedding of the feeds to isolate the performance of the connector interface. These structures may support Thru-Reflect-Line, the 2x thru procedure, or different de-embedding method. The de-embedding structures' signal launch and traces must match those of the test fixture.
- The baseboard, and Add-in Card must be on the same PCB panel during fabrication, and the de-embedding structures must lie on one or both test boards, or on a third, adjacent PCB card. Silkscreen serialization of the test cards during manufacturing may aid in tracking adjacent PCB sets.
- The pinfield must replicate the pin assignments of a x4 connector interface. The pin pairs measured correspond to high speed pairs Tx0, Tx1, and Tx2, as well as Rx0 and Rx1, as shown in Table 6-6. This pinfield will require a x4 connector and x4 card. A baseboard mounting a connector longer than x4 or an Add-in Card longer than x4 may be used but are not required.
- Pins A1/B1 to A11/B11, which lie below the key notch on both sides of the card, may be terminated with an open, short, or an arbitrary impedance. If the Add-in Card is up-plugged into a longer edge connector, such as x8 or x16, the pins beyond A32/B32 may be arbitrarily terminated as well.
- Scattering parameters must be obtained over a range spanning 100 MHz to 10 GHz, with a frequency spacing of no greater than 10 MHz.
- The high-speed pins in Table 6-6 labeled $42.5\ \Omega$ must be terminated with $42.5\ +/-\ 2\ \Omega$ resistors to emulate the termination of an operating high-speed pair. The trace between the high-speed edge-finger or connector pin and the termination must have a characteristic impedance of $42.5\ \Omega$.
- The clock pair, pins A13 and A14, must be terminated single-ended with resistors whose values are $50\ +/-\ 2\ \Omega$. This termination is applied on the baseboard side only; the Add-in Card REFCLK nets are left open circuited at the end of the edge-fingers.
- Compression-fit (bolt-on) PCB mount coaxial connectors are recommended, but not required, for the PCB test ports. The signal launch of the test port connectors must be optimized for lowest return loss across the band of interest.
- Via stubs, both in the test port feeds and in the pinfield, must be avoided.

Table 6-6: Pin Connectivity for the 16.0 GT/s Connector Characterization Board

Pin Number	Signal Assignment	Baseboard Termination	Add-in Card Termination
B12	CLKREQ#	OPEN	R-C TERM
B14	Tx0p	MEASURE	MEASURE
B15	Tx0n	MEASURE	MEASURE
B17	PRSNT2#	OPEN	R-C TERM
B19	Tx1p	MEASURE	MEASURE
B20	Tx1n	MEASURE	MEASURE
B23	Tx2p	MEASURE	MEASURE
B24	Tx2n	MEASURE	MEASURE
B27	Tx3p	42.5 Ω	42.5 Ω
B28	Tx3n	42.5 Ω	42.5 Ω
B30	PWRBRK#	OPEN	R-C TERM
B31	PRSNT2#	OPEN	R-C TERM
A13	REFCLK+	50 Ω	OPEN
A14	REFCLK-	50 Ω	OPEN
A16	Rx0p	MEASURE	MEASURE
A17	Rx0n	MEASURE	MEASURE
A19	MFG	OPEN	R-C TERM
A21	Rx1p	MEASURE	MEASURE
A22	Rx1n	MEASURE	MEASURE
A25	Rx2p	42.5 Ω	42.5 Ω
A26	Rx2n	42.5 Ω	42.5 Ω
A29	Rx3p	42.5 Ω	42.5 Ω
A30	Rx3n	42.5 Ω	42.5 Ω
A32	Reserved	OPEN	R-C TERM

- Test port feeds marked “MEASURE” in the Table 6-6, must be optimized to a characteristic impedance of either 42.5 Ω or 50 Ω . All of the traces on the test baseboard and Add-in Card must be held to the specified characteristic impedance of 42.5 Ω or 50 Ω with a tolerance of $\pm 7\%$.
- For a baseboard mounting press-fit or soldered through-hole mount connectors:
 - The measurement signals shall be launched into the connector pinfield from the bottom of the test fixture baseboard, to prevent any through-hole via stub effects for the connector pins.
 - The connector pinfield through-hole vias must have a 0.70 mm (28 mil) finished hole diameter.
 - The pad (annular ring) must be circular, with a diameter of 1.0 mm (40 mil). For positions representing high speed Tx and Rx signal pairs, the antipad must be 1.5 mm (59 mil) and circular.
 - For positions representing auxiliary (sideband) or Reserved signals, including CLKREQ#, MFG, PRSNT2#, and PWRBRK#; the antipads must be circular, with a diameter of 1.22 mm (48 mil).
 - The traces for the through-hole connector de-embedding structures must lie on the back side of the board, to represent the feed traces on the baseboard and one side of the Add-in Card. An optional second set of de-embedding structures may be placed on the top of the board, to better represent the corresponding feed traces on both sides of the Add-in Card.
 - The measurement signals must be launched into the connector from the bottom of the test fixture baseboard.
 - Two sentry vias (ground vias) must bracket each sideband signal. They must have a drill size of approximately 0.254 mm (10 mil). They must be 180 degrees apart, across the axis of auxiliary signal via. They must lie within 30° to 45° of the direction of the fiber weave, with the via center as the axis, to mitigate conductive anodic filament (CAF) formation between the ground and sideband vias.
- For a baseboard mounting a Surface Mount (SMT) connector:
 - The measurement signals shall be launched into the connector pinfield through topside microstrip on the test fixture baseboard, with no signal vias in the pinfield region.
 - For convenience, to prevent crossed cables during measurement, the SMT baseboard feeds are permitted to lie on the back side of the baseboard PCB. This will require a well-designed through-hole via, located at least 25 mm (98 mil) from the pinfield.
 - Adjacent ground vias must be placed at both ends of each baseboard ground pad.
- For the Add-in Card (AIC):
 - The feed structures must emulate those on the baseboard or have separate de-embedding structures to remove their effects.
 - Mechanical fixtures or other means must be used to ensure full insertion of the card into the slot, and alignment to 90° with the baseboard.
 - Via stubs must be avoided. This may require test port feeds on both sides of the Add-in Card, since both Tx and Rx signals will be characterized.

6.3.6. Signal Integrity Requirements and Test Procedures for 32.0 GT/s Support

An electrical test fixture must be used for evaluating connector signal integrity. The test fixture effects are de-embedded from measurements. Test fixture requirements and recommendations are provided in Section 6.3.6.1. Table 6-7 lists the electrical signal integrity parameters, requirements, and test procedures.

Table 6-7: Signal Integrity Requirements and Test Procedures for 32.0 GT/s Support

Parameter	Procedure	Requirements
Differential Insertion Loss (DDIL)	EIA 364-101 The EIA standard shall be used with the following considerations: 1. The measured differential S-parameter shall be referenced to an 85 Ω differential impedance. 2. The test fixture shall meet the test fixture requirement defined in Section 6.3.6.1. 3. The test fixture effect shall be removed from the measured S-parameters. See Note 1.	$[-0.1 - 0.0875 * f]$ dB for $f \leq 16$ GHz; $[3.5 - 0.3125 * f]$ dB for $16 < f \leq 24$ GHz
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard shall be used with the following considerations: 1. The measured differential S-parameter shall be referenced to an 85 Ω differential impedance. 2. The test fixture shall meet the test fixture requirement in Section 6.3.6.1. 3. The test fixture effect shall be removed. See Note 1.	$[-20 + 0.625 * f]$ dB for $f \leq 16$ GHz; $[-24 + 0.875 * f]$ dB for $16 < f \leq 24$ GHz
Intra-pair Skew	Intra-pair skew must be achieved by design; measurement not required.	5 ps max
Differential Near End Crosstalk (DDNEXT)	EIA 364-90 The EIA standard must be used with the following considerations: 1. The Near-End Crosstalk is the power sum crosstalk with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector, as shown in Figure 6-10. 2. This is a differential crosstalk between a victim differential signal pair and all its adjacent differential signal pairs. The measured differential S-parameter shall be referenced to an 85 Ω differential impedance. 3. If this frequency based DDNEXT requirement is not met, $ccICN_{NEXT}$ must be used to determine the crosstalk energy in the given frequency band using Equation 1 and must be less than the value indicated under the requirements column.	$[1.5 * f - 60]$ dB for $f \leq 10$ GHz; $[(5/6) * f - 53.33]$ dB for $10 < f \leq 24$ GHz; $ccICN_{NEXT} \leq 250 \mu V$ for $f_{max} = 24$ GHz
Differential Far End Crosstalk (DDFEXT)	EIA 364-90 The EIA standard must be used with the following considerations: 1. The Far-End Crosstalk is the power sum crosstalk with respect to all pins 2 pairs away from opposite sides of the connector channel, as shown in Figure 6-11. 2. This is a differential crosstalk between a victim differential signal pair and all the differential signal pins two pairs away. The measured differential S-parameter shall be referenced to an 85 Ω differential impedance. 3. If this frequency based DDFEXT requirement is not met, $ccICN_{FEXT}$ must be used to determine the crosstalk energy in the given frequency band using Equation 2 and must be less than the value indicated under the requirements column.	$[1.5 * f - 60]$ dB for $f \leq 10$ GHz; $[(5/6) * f - 53.33]$ dB for $10 < f \leq 24$ GHz; $ccICN_{FEXT} \leq 250 \mu V$ for $f_{max} = 24$ GHz

Notes: The specified S-parameter requirements are for connector only, not including the test fixture effect.
2x Thru de-embedding, TRL and other methods for calibration and fixture removal are allowed.

Equation 1. Component Contribute Integrated Crosstalk Noise – $ccICN_{NEXT}$

$$ccICN_{NEXT} = \sqrt{\frac{1}{2} df \sum_{k=1}^{N_{max}} \left(\frac{A_{NT}^2}{f_b} \right) \text{sinc}^2 \left(\frac{k \cdot df}{f_b} \right) 10^{(2 \frac{IL_{post-channel}(k)}{10})} \left[\frac{1}{1 + \left(\frac{k \cdot df}{f_t} \right)^4} \right] \left[\frac{1}{1 + \left(\frac{k \cdot df}{f_r} \right)^8} \right] 10^{\frac{MD_{NEXT}(k)}{10}}}$$

Equation 2. Component Contribute Integrated Crosstalk Noise – ccICN_{FEXT}

$$ccICN_{FEXT} = \sqrt{\frac{1}{2} df \sum_{k=1}^{N_{max}} \left(\frac{A_{FT}^2}{f_b} \right) \text{sinc}^2 \left(\frac{k \cdot df}{f_b} \right) 10^{\left(\frac{IL_{pre-channel}(k)}{10} + \frac{IL_{post-channel}(k)}{10} \right)} \left[\frac{1}{1 + \left(\frac{k \cdot df}{f_t} \right)^4} \right] \left[\frac{1}{1 + \left(\frac{k \cdot df}{f_r} \right)^8} \right] 10^{\frac{MDFEXT(k)}{10}}}$$

- $IL_{pre-channel}(k) = -\left(\frac{25}{f_{b/2}}\right) \cdot k \cdot df$, $IL_{post-channel}(k) = -\left(\frac{9.5}{f_{b/2}}\right) \cdot k \cdot df$
- $f_{max} = 24$ GHz, $f_{min} = 10$ MHz, $df = 10$ MHz, $f_b = 32$ GHz
- $A_{FT} = 800$ mVpp, $A_{NT} = 800$ mVpp
- $f_t = 31.53$ GHz, $f_r = 24$ GHz

	Baseboard	Add-in Card		Add-in Card	Baseboard	
B1	PWR	PWR		OPEN	OPEN	A1
B2	PWR	PWR		PWR	PWR	A2
B3	PWR	PWR		PWR	PWR	A3
B4	GND	GND		GND	GND	A4
B5	OPEN	OPEN		OPEN	OPEN	A5
B6	OPEN	OPEN		OPEN	OPEN	A6
B7	GND	GND		OPEN	OPEN	A7
B8	PWR	PWR		OPEN	OPEN	A8
B9	OPEN	OPEN		PWR	PWR	A9
B10	PWR	PWR		PWR	PWR	A10
B11	OPEN	OPEN		OPEN	OPEN	A11
B12	OPEN	42.5 Ω + 1.0 pF term		GND	GND	A12
B13	GND	GND		OPEN	50 Ω term	A13
B14	PETp0	PETp0		OPEN	50 Ω term	A14
B15	PETn0	PETn0		GND	GND	A15
B16	GND	GND		PERp0	PERp0	A16
B17	OPEN	42.5 Ω + 1.0 pF term		PERn0	PERn0	A17
B18	GND	GND		GND	GND	A18
B19	PETp1	PETp1		42.5 Ω + 1.0 pF term	42.5 Ω + 1.0 pF term	A19
B20	PETn1	PETn1		GND	GND	A20
B21	GND	GND		PERp1	PERp1	A21
B22	GND	GND		PERn1	PERn1	A22
B23	PETp2	PETp2		GND	GND	A23
B24	PETn2	PETn2		GND	GND	A24
B25	GND	GND		PERp2	PERp2	A25
B26	GND	GND		PERn2	PERn2	A26
B27	PETp3	PETp3		GND	GND	A27
B28	PETn3	PETn3		GND	GND	A28
B29	GND	GND		PERp3	PERp3	A29
B30	42.5 Ω + 1.0 pF term	42.5 Ω + 1.0 pF term		PERn3	PERn3	A30
B31	42.5 Ω + 1.0 pF term	42.5 Ω + 1.0 pF term		GND	GND	A31
B32	GND	GND		OPEN	OPEN	A32

Figure 6-10. Differential Near End Crosstalk Victim-Aggressor Pattern for 32.0 GT/s Operation

	Baseboard	Add-in Card		Add-in Card	Baseboard	
B1	PWR	PWR		OPEN	OPEN	A1
B2	PWR	PWR		PWR	PWR	A2
B3	PWR	PWR		PWR	PWR	A3
B4	GND	GND		GND	GND	A4
B5	OPEN	OPEN		OPEN	OPEN	A5
B6	OPEN	OPEN		OPEN	OPEN	A6
B7	GND	GND		OPEN	OPEN	A7
B8	PWR	PWR		OPEN	OPEN	A8
B9	OPEN	OPEN		PWR	PWR	A9
B10	PWR	PWR		PWR	PWR	A10
B11	OPEN	OPEN		OPEN	OPEN	A11
B12	OPEN	42.5 Ω + 1.0 pF term		GND	GND	A12
B13	GND	GND		OPEN	50 Ω term	A13
B14	PETp0	PETp0		OPEN	50 Ω term	A14
B15	PETn0	PETn0		GND	GND	A15
B16	GND	GND		PERp0	PERp0	A16
B17	OPEN	42.5 Ω + 1.0 pF term		PERn0	PERn0	A17
B18	GND	GND		GND	GND	A18
B19	PETp1	PETp1		42.5 Ω + 1.0 pF term	42.5 Ω + 1.0 pF term	A19
B20	PETn1	PETn1		GND	GND	A20
B21	GND	GND		PERp1	PERp1	A21
B22	GND	GND		PERn1	PERn1	A22
B23	PETp2	PETp2		GND	GND	A23
B24	PETn2	PETn2		GND	GND	A24
B25	GND	GND		PERp2	PERp2	A25
B26	GND	GND		PERn2	PERn2	A26
B27	PETp3	PETp3		GND	GND	A27
B28	PETn3	PETn3		GND	GND	A28
B29	GND	GND		PERp3	PERp3	A29
B30	42.5 Ω + 1.0 pF term	42.5 Ω + 1.0 pF term		PERn3	PERn3	A30
B31	42.5 Ω + 1.0 pF term	42.5 Ω + 1.0 pF term		GND	GND	A31
B32	GND	GND		OPEN	OPEN	A32

**Figure 6-11. Differential Far End Crosstalk Victim-Aggressor Pattern
for 32.0 GT/s Operation**

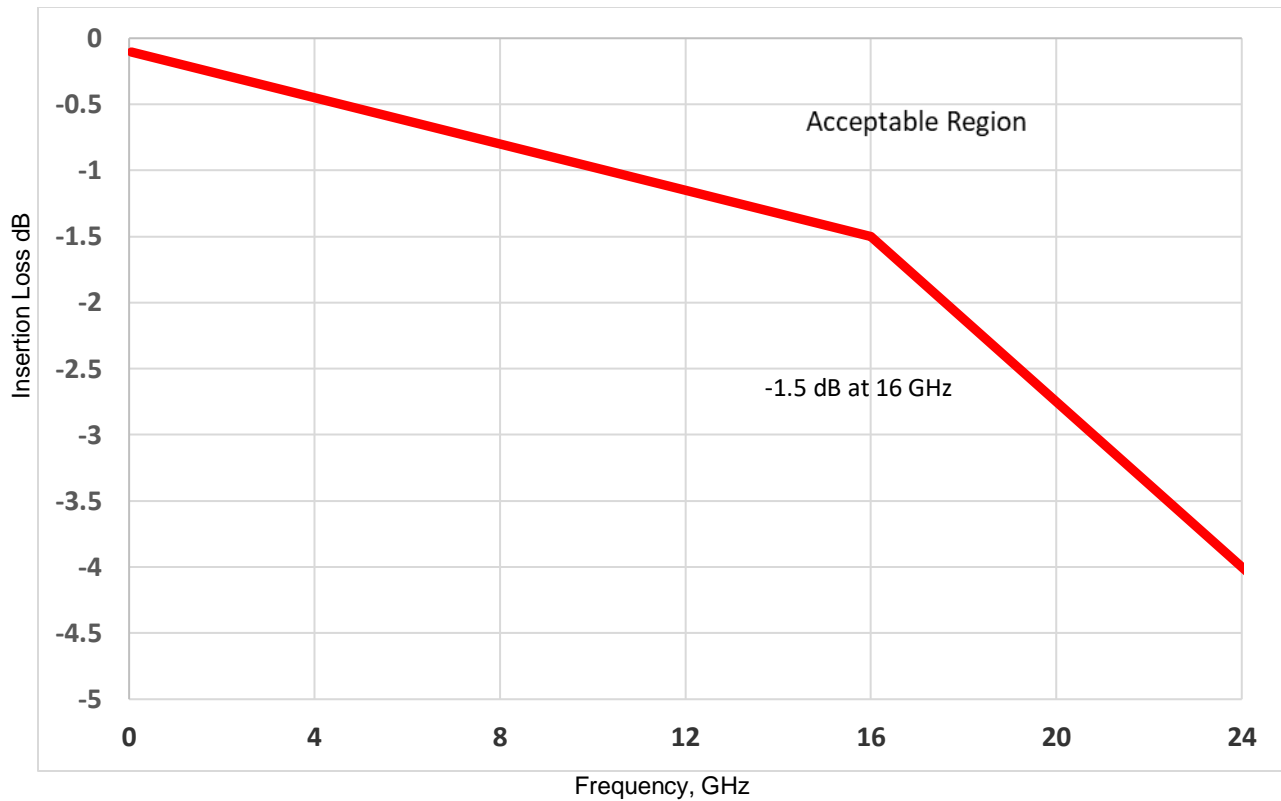


Figure 6-12. Differential Insertion Loss Limits for 32.0 GT/s Operation

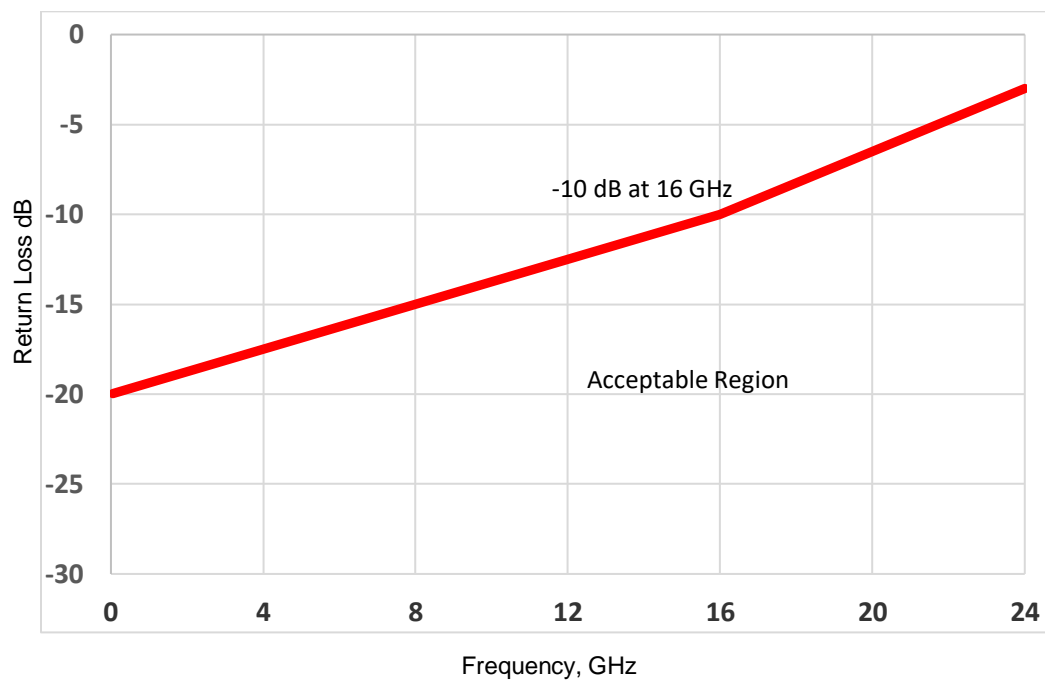


Figure 6-13. Differential Return Loss Limits for 32.0 GT/s Operation

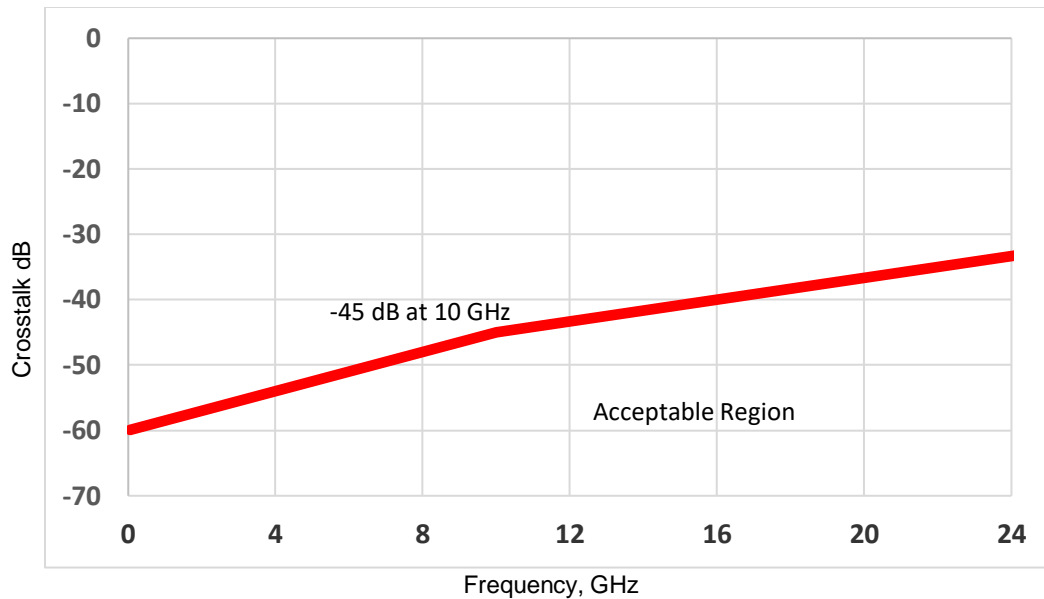


Figure 6-14. Differential Near/Far End Crosstalk Limits for 32.0 GT/s Operation

6.3.6.1 Test Fixture Requirements

A test fixture for connector S-parameter measurement must be designed and built to the following:

- The test fixture used for measuring S-parameter will comprise a baseboard and mating Add-in Card fabricated from the same PCB panel. The total thickness of the boards, measured across the Add-in Card edge-fingers, must be 1.57 mm (62 mil).
- The PCB test fixture must be an FR-4 based material, or of a lower loss material with a relative permittivity between 3.3 and 3.6 at 1.0 GHz. Dielectric loss factor is not specified.
- The interconnect traces on all boards must be routed uncoupled (single-ended) where possible. Some method of mitigating fiber weave effects must be applied. This can include off-axis routing or board rotation on the PCB panel.
- The trace lengths between the connector and measurement port must be minimized. The maximum trace length must not exceed 48 mm (1.9 inches). The trace lengths between the connector and measurement port on the test baseboard and Add-in Card must be matched within 0.5 mil. The edge-finger pad is not counted as Add-in Card PCB trace; it is considered part of the connector interface.
- Separate PCB structures must be included to support de-embedding of the feeds to isolate the performance of the connector interface. These structures may support Thru-Reflect-Line, the 2x thru procedure, or a different de-embedding method. The de-embedding structures' signal launch and traces must match those of the test fixture.
- The baseboard and Add-in Card must be on the same PCB panel during fabrication, and the de-embedding structures must lie on one or both test boards, or on a third, adjacent PCB card. Silkscreen serialization of the test cards during manufacturing may aid in tracking adjacent PCB sets.
- The pinfield must replicate the pin assignments of a x4 connector interface. The pin pairs measured correspond to high-speed pairs Tx0, Tx1, and Tx2, as well as Rx0 and Rx1, as shown in Table 6-8. This pinfield will require a x4 connector and x4 card. A baseboard mounting a connector longer than x4 or an Add-in Card longer than x4 may be used but are not required.

- Pins A1/B1 to A11/B11, which lie below the key notch on both sides of the card, may be terminated with an open, short, or an arbitrary impedance. If the Add-in Card is up-plugged into a longer edge connector, such as x8 or x16, the pins beyond A32/B32 may be arbitrarily terminated as well.
- Scattering parameters must be obtained over a range spanning 100 MHz to 24 GHz, with a frequency spacing of no greater than 10 MHz.

Table 6-8. Pin Connectivity for the 32.0 GT/s Connector Characterization Board

Pin Number	Signal Assignment	Baseboard Termination	Add-in Card Termination
B12	CLKREQ#	R-C TERM	R-C TERM
B14	Tx0p	MEASURE	MEASURE
B15	Tx0n	MEASURE	MEASURE
B17	PRSNT2#	R-C TERM	R-C TERM
B19	Tx1p	MEASURE	MEASURE
B20	Tx1n	MEASURE	MEASURE
B23	Tx2p	MEASURE	MEASURE
B24	Tx2n	MEASURE	MEASURE
B27	Tx3p	MEASURE	MEASURE
B28	Tx3n	MEASURE	MEASURE
B30	PWRBRK#	R-C TERM	R-C TERM
B31	PRSNT2#	R-C TERM	R-C TERM
A13	REFCLK+	50 Ω	OPEN
A14	REFCLK-	50 Ω	OPEN
A16	Rx0p	MEASURE	MEASURE
A17	Rx0n	MEASURE	MEASURE
A19	Reserved	R-C TERM	R-C TERM
A21	Rx1p	MEASURE	MEASURE
A22	Rx1n	MEASURE	MEASURE
A25	Rx2p	MEASURE	MEASURE
A26	Rx2n	MEASURE	MEASURE
A29	Rx3p	42.5 Ω	42.5 Ω
A30	Rx3n	42.5 Ω	42.5 Ω
A32	Reserved	R-C TERM	R-C TERM

- The high-speed pins in Table 6-8 labeled 42.5 Ω must be terminated with 42.5 \pm 2 Ω resistors to emulate the termination of an operating high-speed pair. The trace between the high-speed edge-finger or connector pin and the termination must have a characteristic impedance of 42.5 Ω .
- The clock pair, pins A13 and A14, must be terminated single-ended with resistors whose values are 50 \pm 2 Ω . This termination is applied on the baseboard side only; the Add-in Card REFCLK nets are left open-circuited at the end of the edge-fingers.
- Compression-fit (bolt-on) PCB mount coaxial connectors are recommended, but not required, for the PCB test ports. The signal launch of the test port connectors must be optimized for lowest return loss across the band of interest.
- Via stubs, both in the test port feeds must be avoided.

- Test port feeds marked “MEASURE” in the Table 6-8, must be optimized to a characteristic impedance of either 42.5 Ω or 50 Ω . All of the traces on the test baseboard and Add-in Card must be held to the specified characteristic impedance of 42.5 Ω or 50 Ω with a tolerance of $\pm 7\%$.
- All system boards must use a Surface Mount (SMT) connector for 32.0 GT/s operation:
 - The measurement signals shall be launched into the connector pinfield through topside microstrip on the test fixture baseboard, with no signal vias in the pinfield region.
 - For convenience, to prevent crossed cables during measurement, the SMT baseboard feeds are permitted to lie on the back side of the baseboard PCB. This will require a well-designed through-hole via, located at least 25 mm (98 mil) from the pinfield.
 - Adjacent ground vias must be placed at both ends of each baseboard ground pad.
- For the Add-in Card (AIC):
 - The feed structures must emulate those on the baseboard or have separate de-embedding structures to remove their effects.
 - Mechanical fixtures or other means must be used to ensure full insertion of the card into the slot, and alignment to 90° with the baseboard.
 - Via stubs must be avoided. This may require test port feeds on both sides of the Add-in Card since both Tx and Rx signals will be characterized.
 - There must be an inner layer ground plane under edge-fingers in the high-speed region comprising pins A12/B12 and beyond. This requirement applies to both sides of the Add-in Card, so a symmetric pair of shielding planes will be used.
 - The inner layer ground plane must extend the full length of the edge-finger region from the main routing area of the board.
 - The inner layer ground plane must lie at a depth of 0.52 mm (20.5 mil) or deeper beneath the edge-finger copper pads on the surface of the PCB.
 - There must be a row of plated vias connected to the inner layer ground plane along the bottom of the edge-fingers in the high-speed region comprising pins A12/B12 and beyond. These are collectively known as Fingertip South Vias.
 - The vias must be plated through-holes (PTH) and may be shared among ground pads on both faces of the Add-in Card.
 - Ground vias must be joined in the “I bar” with surface metal, and should be center aligned with the gap between the pads, offset from the edge-fingers by 0.50 mm.
 - A lateral ground bar must be implemented to join all of the Fingertip South Vias on the first inner layer (N-1) on each side of the board (Metal 2, for example).

6.4. Connector Environmental and Other Requirements

6.4.1. Environmental Requirements

Connector environmental tests shall follow *EIA-364-1000.01*.

The test groups/sequences and durations shall be derived from the following requirements:

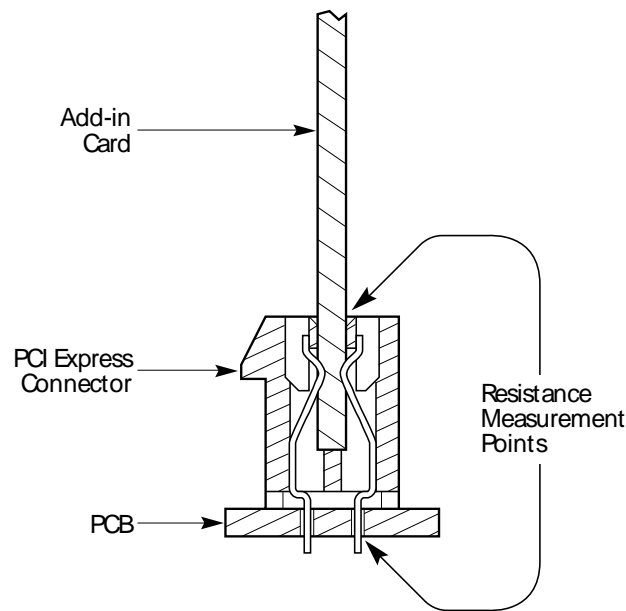
- Durability (mating/unmating) rating of 50 cycles
- Field temperature: 65 °C
- Field life: seven years

Since the connector defined in Section 6.2 has far more than 0.127 mm wipe length, Test Group 6 in *EIA-364-1000.01* is not required. Test Group 7 in *EIA-364-1000.01* is optional since the durability cycles is ≤ 50 . The temperature life test duration and the mixed flowing gas test duration values are derived from *EIA 364-1000.01* based on the field temperature, using simple linear interpolation. Table 6-9 lists these values.

Table 6-9: Test Durations

Test	Duration/Temperature
Temperature Life	168 hours at 105 °C
Temperature Life (preconditioning)	92 hours at 105 °C
Mixed Flowing Gas	10 days

The low-level contact resistance (LLCR) is required to be 30 mΩ or less, initially. The contact resistance measurement points shall include the solder tail and the contact-mating interface, as illustrated in Figure 6-15. The resistance change, which is defined as the change in LLCR between the reading after stress and the initial reading, shall not exceed the value that is to be specified by each OEM to best suit their needs.



OM1476

Figure 6-15: Contact Resistance Measurement Points

To be sure that the environmental tests measure the stability of the connector, the Add-in Cards used shall have edge-finger tabs with a minimum plating thickness of 30 microinches of gold over 50 microinches of nickel for the environmental test purpose only. Furthermore, it is highly desirable that testing gives an indication of the stability of the connector when Add-in Cards at the lower and upper limit of the card thickness requirement are used. In any case, both the edge tab plating thickness and the card thickness shall be recorded in the environmental test report.

6.4.2. Mechanical Requirements

Table 6-10 lists the mechanical parameters and requirements. The sample size follows *EIA-364-1000.01*.

Table 6-10: Mechanical Test Procedures and Requirements

Test Description	Procedure	Requirement
Visual and dimensional inspections	EIA 364-18 Visual, dimensional, and functional per applicable quality inspection plan	Meets product drawing requirements
Insertion force	EIA 364-13 Measure the force necessary to mate the connector assemblies at a maximum rate of 12.5 mm (0.492 inches) per minute, using a steel gauge 1.70 mm thick with a tolerance +0.00, -0.01 mm.	1.15 N maximum per contact pair
Removal force	EIA 364-13 Measure the force necessary to unmate the connector assemblies at maximum rate of 12.5 mm (0.492 inches) per minute, using a steel gauge 1.44 mm thick with a tolerance +0.01, - 0.00 mm.	0.15 N minimum per contact pair

6.4.3. Current Rating Requirement

Table 6-11 lists the contact current rating requirement and test procedure.

Table 6-11: End of Life Current Rating Test Sequence

Test Order	Test	Procedure	Condition	Requirement
1	Contact current rating	EIA 364-70 method 2 The sample size is a minimum of three mated connectors. The sample shall be soldered on a board with the appropriate footprint. Wire the nine power pins (B1, B2, B3, A2, A3, B8, A9, A10, and B10) and the nine nearest ground pins (A4, B4, B7, A12, B13, A15, B16, B18, and A18) in a series circuit. The mated Add-in Card is included in this circuit. The Add-in Card shall have 1 oz. copper traces and its mating geometry shall conform to the applicable PCI Express drawings. A thermocouple of 30 AWG or less shall be placed on the card edge-finger pad (pins B2 and A9) as close to the mating contact as possible. Conduct a temperature rise vs. current test.	Mated	1.1 A per pin minimum The temperature rise above ambient shall not exceed 30 °C. The ambient condition is still air at 25 °C.

6.4.4. Additional Considerations

Table 6-12 lists the additional requirements.

Table 6-12: Additional Requirements

Parameter	Procedure	Requirement
Flammability	UL94V-1 minimum	Material certification or certificate of compliance required with each lot to satisfy the Underwriters Laboratories follow-up service requirements.
Lead-free soldering		Connector must be compatible with lead free soldering process.

This specification does not attempt to define the connector requirements that are considered application specific. It is up to the users and their connector suppliers to determine if additional requirements shall be added to satisfy the application needs. The system level shock and vibration tests are considered application-specific because results will depend on card weight and size, chassis stiffness, and retention mechanisms, as well as the connector. Therefore, those tests are not specified in the connector specification. It will be up to each system OEM to decide how the shock and vibration tests shall be done.

7. PCI Express 2x3 Auxiliary Power Connector Definition

This chapter defines the PCI Express 2x3 (6-position) auxiliary power connector and cable assembly to support higher power Add-in Cards.

7.1. 2x3 Power Connector System Performance Requirements

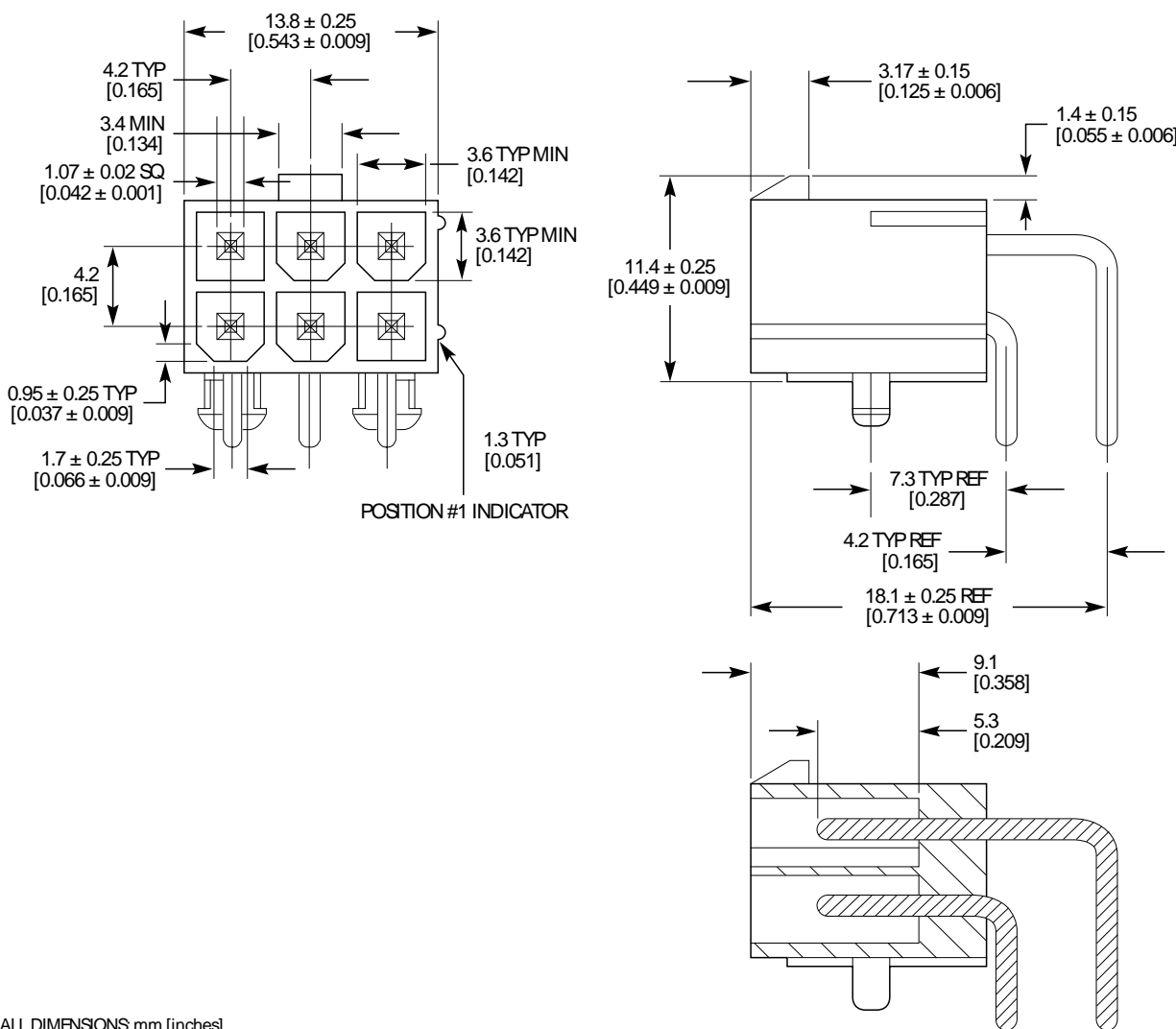
The 2x3 power connector system performance requirements are as follows:

- Current Rating: 8.0 A/pin/position maximum to a 30 °C T-Rise above ambient temperature conditions at +12 VDC, all six contacts energized.
- Mated Connector Retention: 30.00 N minimum when plug pulled axially.

7.2. 2x3 PCB Header

7.2.1. 2x3 Right Angle Through-hole PCB Header

Figure 7-1 shows the details of a 2x3 Right Angle (R/A) PCB Header.



ALL DIMENSIONS mm [inches]

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Figure 7-1: 2x3 Right Angle Through-hole PCB Header**2x3 Right Angle Through-hole PCB Header:**

1. Housing Material: Thermoplastic
2. Pin Contact Base Material: Brass alloy or equivalent
3. Pin Contact Plating: Sn alloy
4. Connector Mechanical Keying: Per Figure 7-1

7.2.2. 2x3 Right Angle Through-hole Header Recommended PCB Footprint

Figure 7-2 shows the recommended PCB footprint for a 2x3 Right Angle through-hole header.

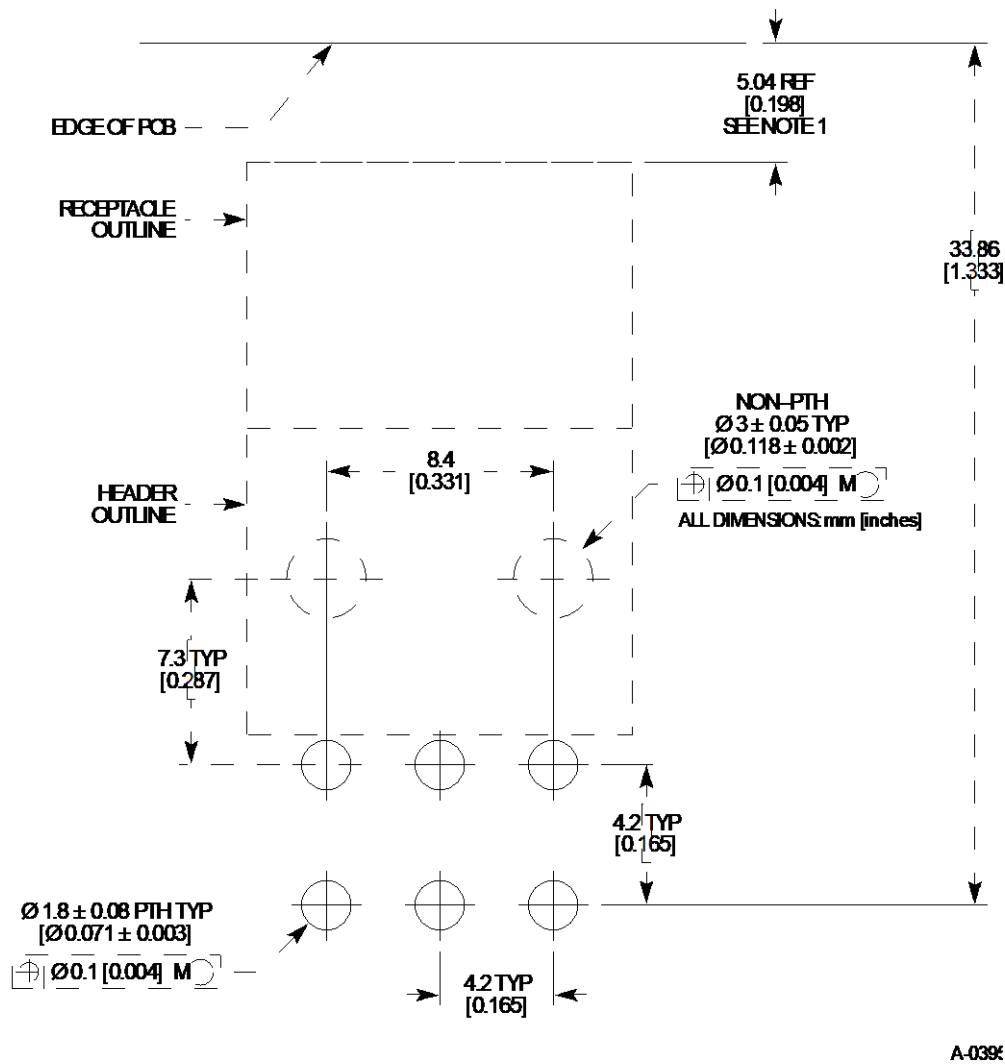
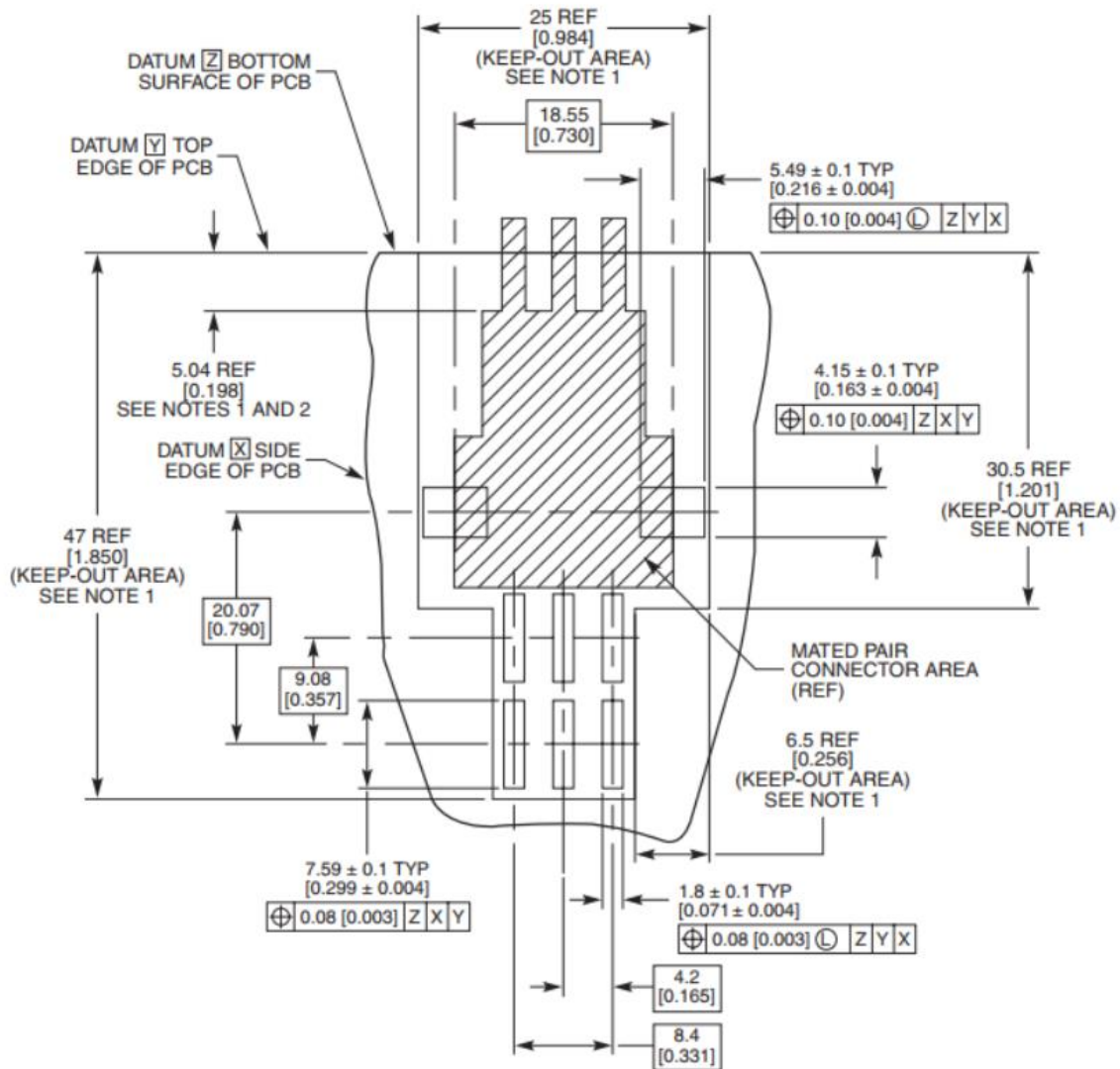


Figure 7-2: 2x3 Right Angle Through-hole Header Recommended PCB Footprint

7.2.4. 2x3 Right Angle SMT Header Recommended PCB Footprint

Figure 7-4 shows the recommended PCB footprint for a 2x3 Right Angle SMT header.



NOTES:

1. KEEP-OUT DIMENSIONS SHOWN ARE BASED ON R/A HEADER PLACEMENT RELATIVE TO TOP EDGE OF PCB AND ARE FOR REFERENCE PURPOSES ONLY.
2. THIS RECOMMENDED PCB FOOTPRINT LOCATION ON THE GRAPHICS CARD IS BASED ON A SPECIFIC CONNECTOR PLACEMENT OF 5.04 mm FROM THE TOP EDGE OF THE PCB TO THE BACK SURFACE OF THE MATING CABLE ASSEMBLY HOUSING AS SHOWN ABOVE AND IS FOR REFERENCE PURPOSES ONLY.
3. THIS RECOMMENDED PCB FOOTPRINT IS BASED ON THE R/A SMT HEADER CONFIGURATION SHOWN IN FIGURE 5. MODIFICATIONS TO THE R/A SMT HEADER REFERENCE DIMENSIONS (FIGURE 5) MAY REQUIRE A NEW PCB FOOTPRINT DESIGN.
4. ALL DIMENSIONS: mm [inches]

A-0397

For Header configuration (Note 3), see Figure 7-3.

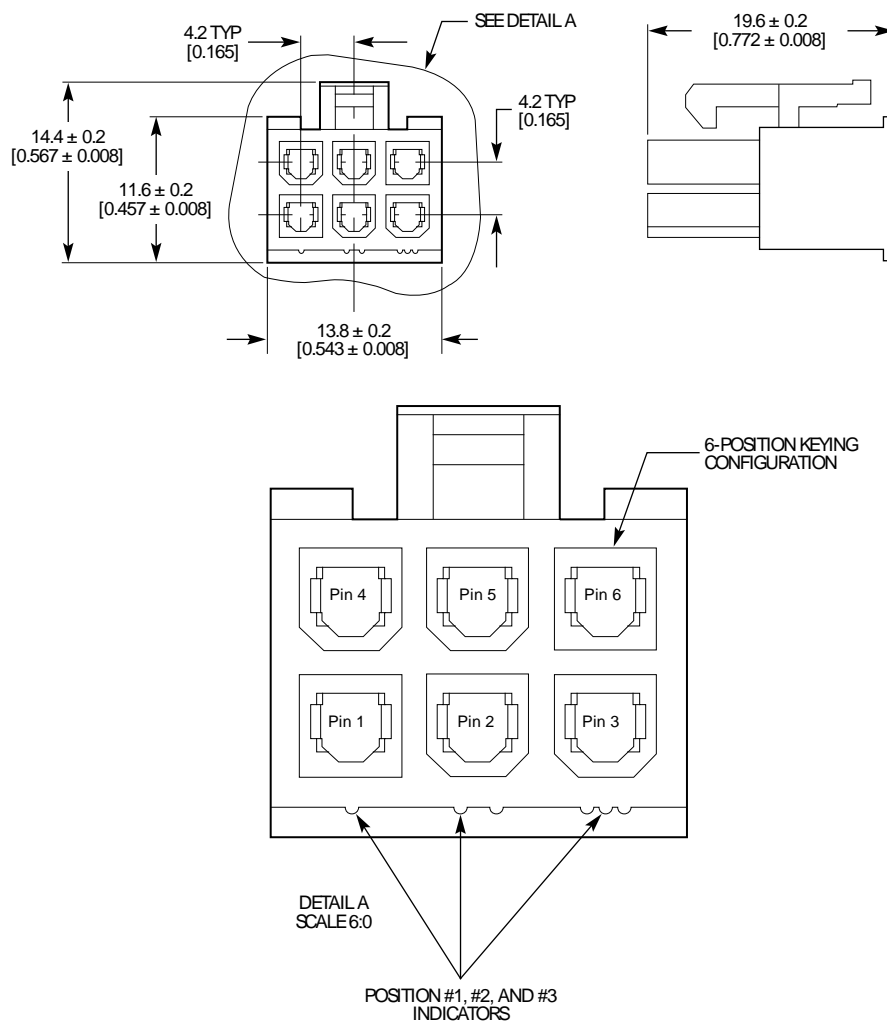
Figure 7-4: 2x3 SMT Header Recommended PCB Footprint

7.3. 2x3 Cable Assembly

Figure 7-5 shows the cable connector housing.

Cable Assembly Contact and Housing Details:

- Housing Material: Thermoplastic
- Pin Contact Base Material: Brass alloy or equivalent
- Pin Contact Plating: Sn alloy
- Connector Mechanical Keying: See Figure 7-5
- See Table 7-1 for pinout



ALL DIMENSIONS mm [inches]

A-0398

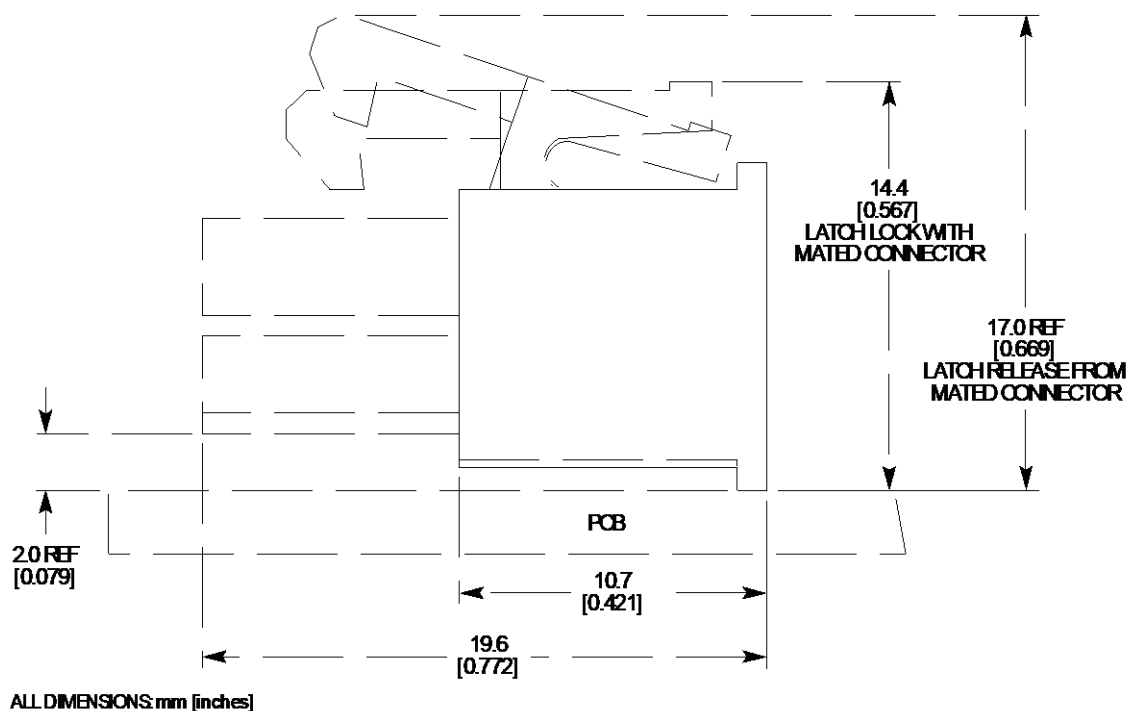
Figure 7-5: Cable Connector Housing

Cable Assembly Wire Details:

- Wire Size: 18 AWG

7.4. Connector Mating-Unmating Keepout Area (Latch Lock Release)

The connector mating-unmating keepout area is specified in Figure 7-6.



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Figure 7-6: Connector Mating-Unmating Keepout Area (Latch Lock Release)

7.5. 2x3 Power Connector System Pin Assignment

Figure 7-7 and Table 7-1 show the pin-out for the PCI Express 2x3 auxiliary power connector.

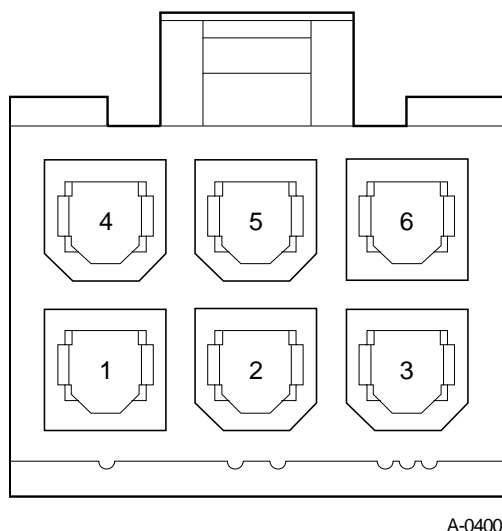


Figure 7-7: 2x3 Auxiliary Power Connector

Table 7-1: 2x3 Auxiliary Power Connector Pin-out

Pin	Signal
1	+12 V
2	+12 V
3	+12 V
4	Ground
5	Sense
6	Ground



IMPLEMENTATION NOTE

2x3 Auxiliary Power Connector Sense Pin

The Sense pin on the 2x3 auxiliary power connector must be connected to ground either directly in the power supply or via a jumper to an adjacent ground pin in the connector. This pin is used by a PCI Express 2x3 150 W/225 W/300 W Add-in Card to detect if the 2x3 auxiliary power connector is attached.

7.6. Additional Considerations

Table 7-2 lists the additional requirements for the 2x3 auxiliary power connector.

Table 7-2: 2x3 Auxiliary Power Connector Additional Requirements

Parameter	Procedure	Requirement
Flammability	UL94V-1 minimum	Material certification or certificate of compliance is required with each lot to satisfy the Underwriters Laboratories follow-up service requirements.
Lead-free soldering		Connector must be compatible with lead free soldering process.
Connector Color		The color of the connector must be black. Exceptions will be made for color coding schemes that call for a different color of this connector.

8. PCI Express 2x4 Auxiliary Power Connector Definition

This chapter defines the PCI Express 2x4 auxiliary power connector and cable assembly.

For backward compatibility, the 2x3 power connector plug can be inserted into the 2x4 connector header. The 2x4 header is keyed such that the 2x3 connector plug needs to be properly aligned to plug in. Based on the sense pins in the 2x4 plug, a 225 W/300 W card with a 2x4 header can detect whether a 2x4 or a 2x3 plug is inserted. The 225 W/300 W card can then draw the appropriate power correspondingly.

The 2x4 connector plug must not be inserted into the 2x3 connector header and is physically prevented from doing so. A dongle must be used for this purpose.

Figure 8-1, Figure 8-2, and Figure 8-3 show the described auxiliary power connector mating scenarios.

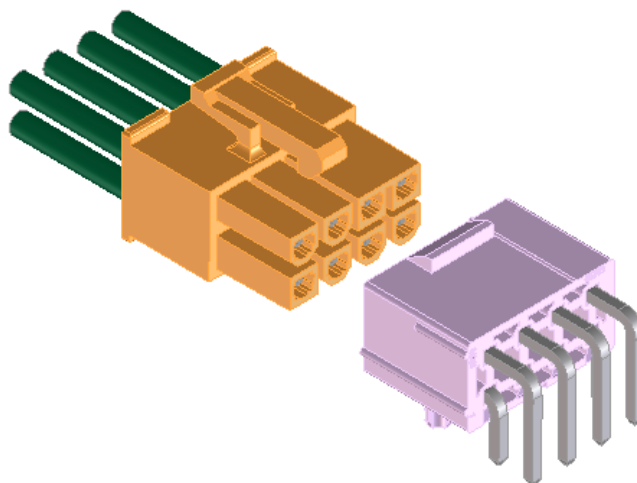


Figure 8-1: 2x4 Plug Mating with a 2x4 Header

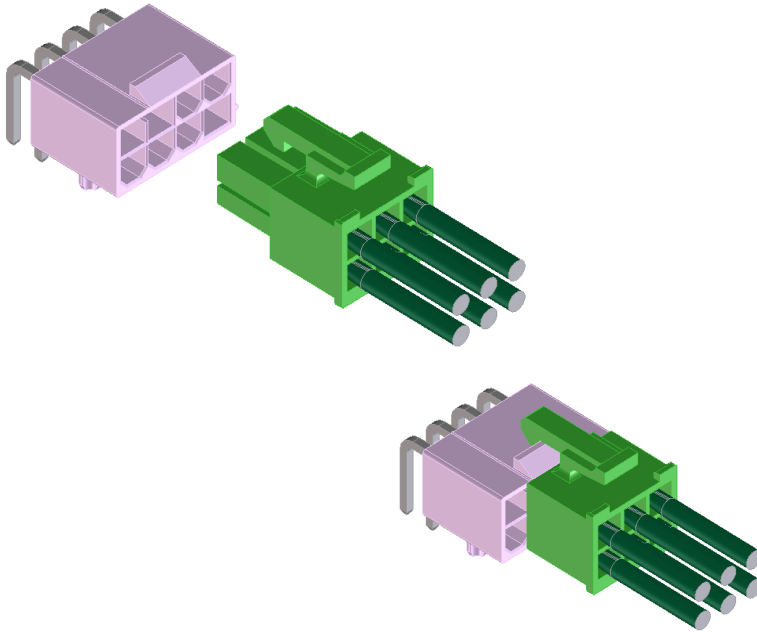


Figure 8-2: 2x3 Cable Plug Mating with a 2x4 PCB Header

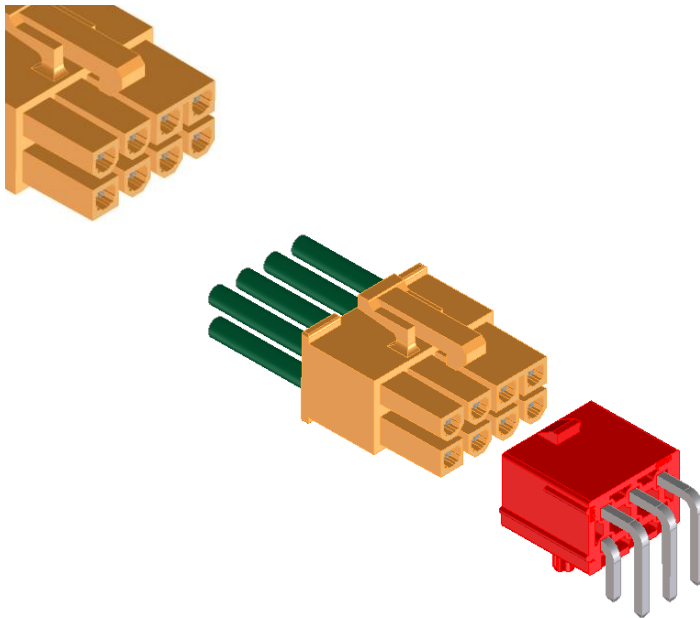


Figure 8-3: 2x4 Cable Plug is Physically Prevented from Mating with a 2x3 PCB Header

8.1. 2x4 Auxiliary Power Connector Performance Requirements

The auxiliary power connector performance requirements are as follows:

- Current Rating: 7.0 A per pin/position maximum to a 30 °C T-Rise above ambient temperature conditions at +12 VDC with all eight contacts energized
- Mated Connector Retention: 30.00 N minimum when plug pulled axially



IMPLEMENTATION NOTE

Auxiliary Power Connector Current Rating

System integrators should ensure that the contacts used in an auxiliary power connector are of the correct rating to meet the 7.0 A requirement. Appropriate derating practices should be used.

8.2. 2x4 Connector Header

8.2.1. Through-Hole Connector Drawing

Figure 8-4 shows the details of a 2x4 (eight-position), Right Angle (R/A) through-hole connector.

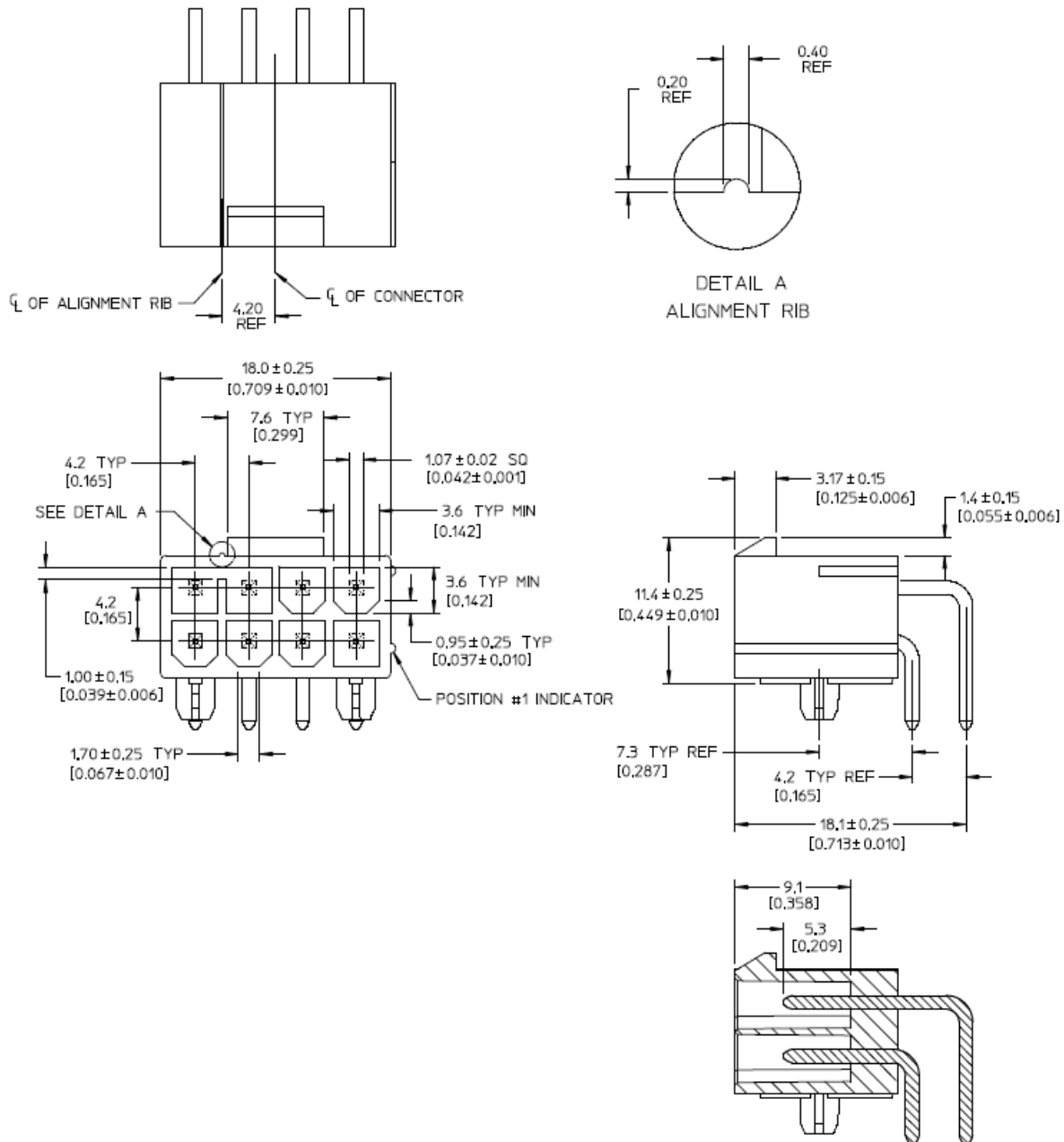
2x4 R/A Through-Hole Header:

- Housing Material: Thermoplastic
- Pin Contact Base Material: Brass Alloy or equivalent
- Pin Contact Plating: Sn Alloy
- An alignment rib is defined (detail A) to help guide the mating with a 2x3 plug.



IMPLEMENTATION NOTE

Though not defined in this specification, a vertical header, in which the mating cable plug is perpendicular to the Add-in Card, is also allowed. Add-in Card manufacturers can work with their connector vendors to enable such a connector.

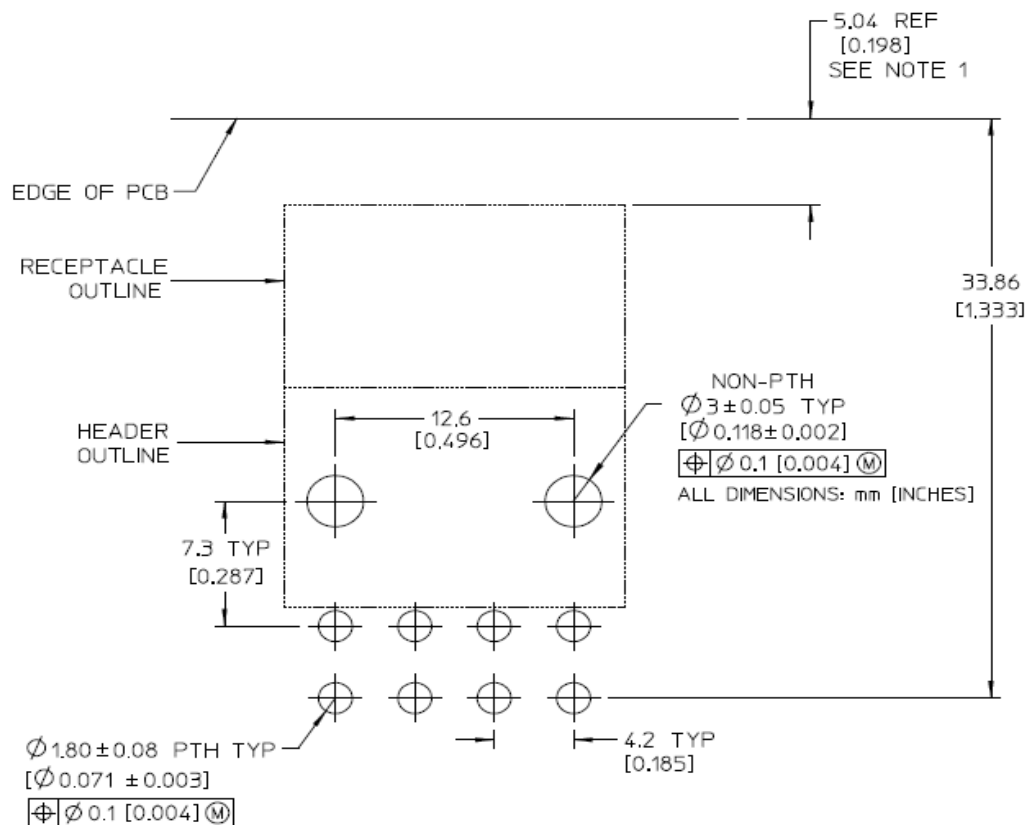


Note: All dimensions are in mm[inches].

Figure 8-4: 2x4 Right Angle Through-Hole Header Drawing

8.2.2. 2x4 R/A Through-Hole Header PCB Footprint

Figure 8-5 shows the recommended PCB footprint for the 2x4 Right Angle through-hole header.

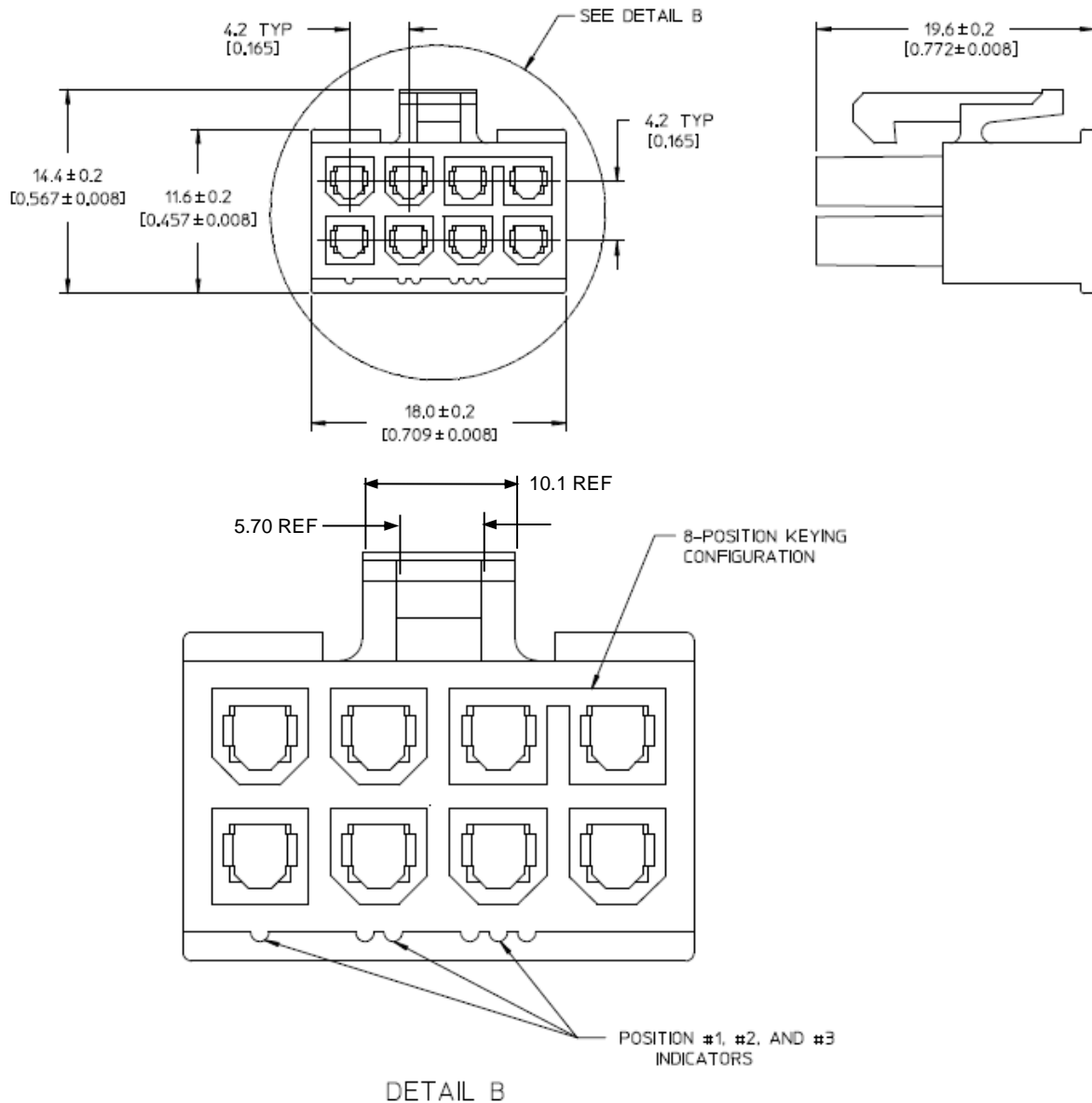


Note: All dimensions are in mm[inches].

Figure 8-5: 2x4 Right Angle Through-Hole Header Recommended PCB Footprint

8.3. Cable Assembly

Figure 8-6 shows the 2x4 cable plug connector housing.



Note: All dimensions are in mm[inches].

Figure 8-6: 2x4 Cable Plug Connector Housing

Cable Assembly Contact and Housing Details:

- Housing Material: Thermoplastic; Note that this connector has unique mechanical keying to avoid wrongful insertion of cable plug meant for different types of connectors. See Figure 8-7 for mechanical keying details.
- Pin Contact Base Material: Brass alloy or equivalent
- Pin Contact Plating: Sn alloy

Cable Assembly Wire Details:

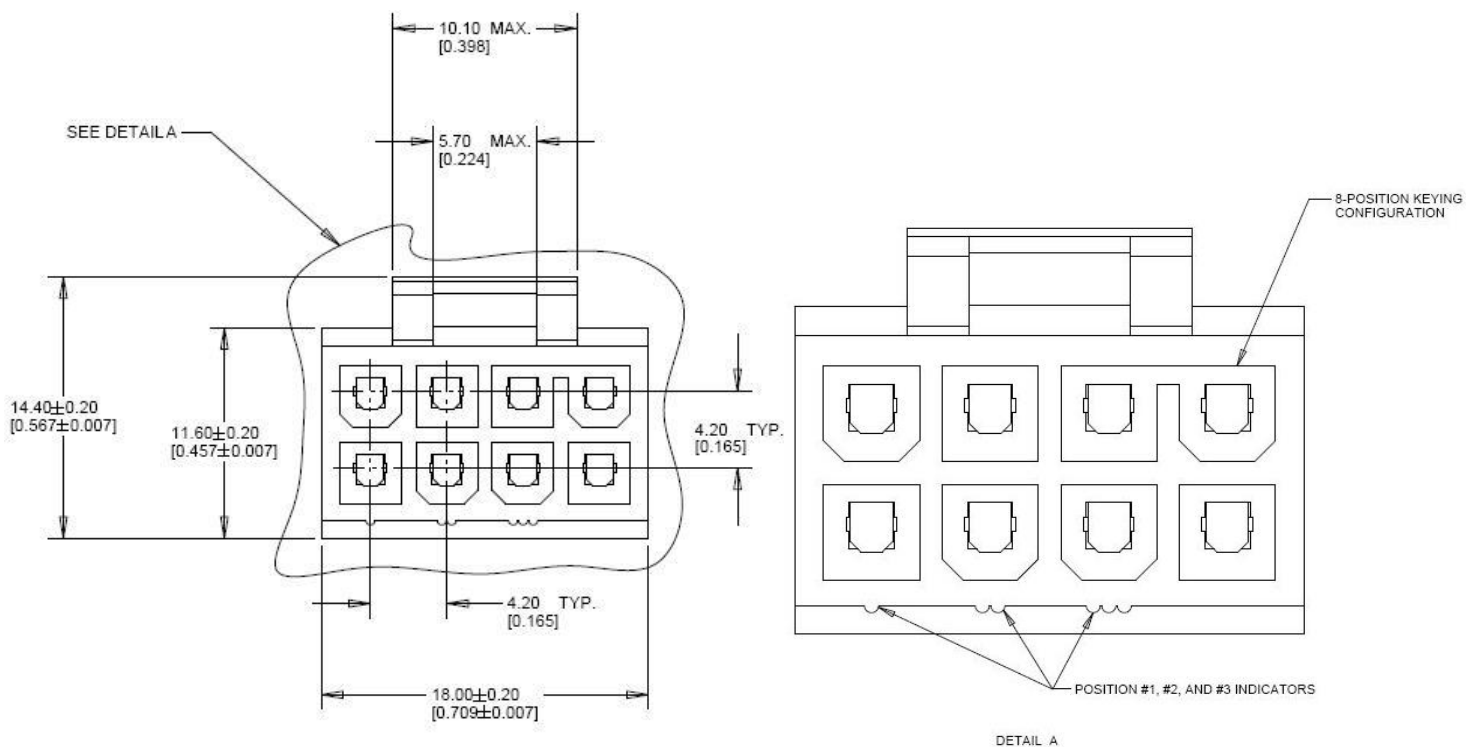
- Wire Size: 18 AWG

**IMPLEMENTATION NOTE****Modular Plug Connector Assembly**

A 2x4 plug connector can be designed with a 2x3 plug module and a 2 x 1 plug module to form a 2x4 modular plug connector such that it can be plugged into a 2x4 or 2x3 header. Cable assembly vendors should design the Latch Lock Hook and Release Handle with the dimensions defined in Note: All dimensions are in mm[inches].

Figure 8-7 to ensure that the plug connector locks securely when plugged into a 2x4 or a 2x3 header. The rest of the dimensions are the same as shown in Note: All dimensions are in mm[inches].

Figure 8-6.

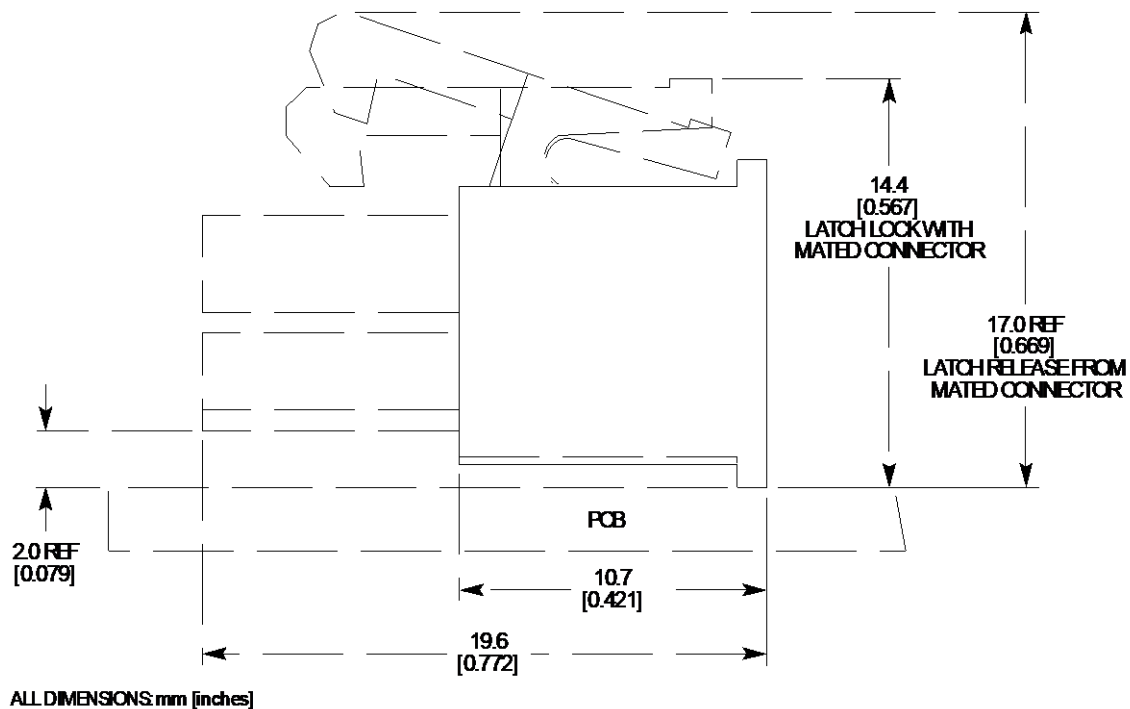


Note: All dimensions are in mm[inches].

Figure 8-7: Modular Plug Connector Housing

8.4. Connector Mating-Unmating Keepout Area (Latch Lock Release)

The connector mating-unmating keepout area is specified in Figure 8-8.



A-0396

Figure 8-8: Connector Mating-Unmating Keepout Area (Latch Lock Release)

8.5. 2x4 Auxiliary Power Connector System Pin Assignment

Figure 8-9 and Figure 8-10 show the pin-out for the 2x4 auxiliary power connector.

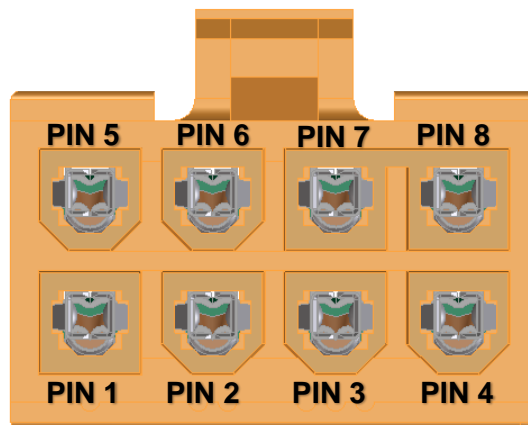


Figure 8-9: 2x4 Auxiliary Power Connector Plug Side Pin-out

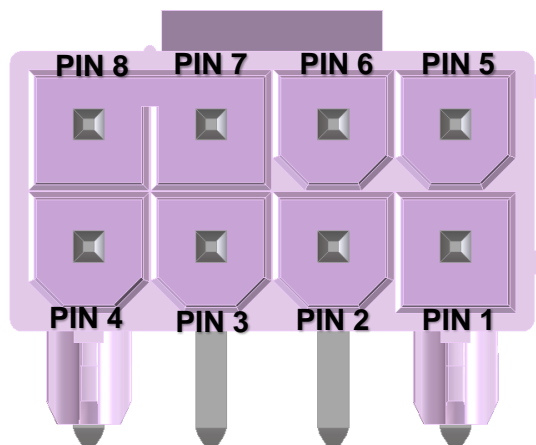


Figure 8-10: 2x4 Auxiliary Power Connector Header Side Pin-out

Table 8-1 and Table 8-2 show the 2x4 pin-out assignments. A 225 W/300 W card with a 2x4 connector header, decodes the sense coding to determine how much power to draw from the 2x4 auxiliary power connector.

Table 8-1: 2x4 Auxiliary Power Connector Pin Assignment

Pin	Signal
1	+12 V
2	+12 V
3	+12 V
4	Sense1
5	Ground
6	Sense0
7	Ground
8	Ground

Table 8-2: Sense Pins Decoding by an Add-in Card

Sense1	Sense0	Comment
Ground	Ground	A 2x4 connector is plugged into the card. The card can draw up to 150 W from the auxiliary power connector (see Section 5.2 for additional limits).
Ground	Open	Reserved
Open	Ground	A 2x3 connector is plugged into the card. The card can only draw up to 75 W from the auxiliary power connector (see Section 5.2 for additional limits).
Open	Open	No auxiliary power connector is plugged in.

For a sense pin that needs to be grounded, it must be connected to ground either directly in the power supply or via a jumper to an adjacent ground pin in the connector. A PCI Express 225 W/300 W card uses sense pins to detect how much power to draw from the 2x3 or 2x4 connector.

A 2x4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.

For informational purposes, Figure 8-11 shows the 2x3 connector pin-out. Table 8-3 shows how the pins are mapped when a 2x3 plug is inserted into a 2x4 header.

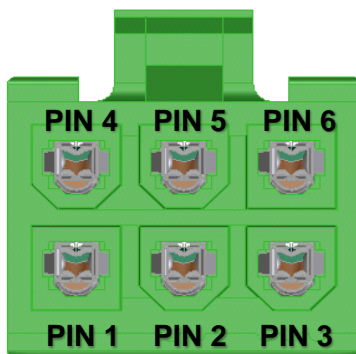
**Figure 8-11: 2x3 Connector Pin-out**

Table 8-3: 2x3 Plug to 2x4 Header Pin Mapping

2x3 Plug	2x4 Header	Signal
1	1	+12 V
2	2	+12 V
3	3	+12 V
NA	4	Sense1
4	5	Ground
5	6	Sense0
6	7	Ground
NA	8	Ground

8.6. PCI Express 2x4 Power Connector Additional Considerations

Table 8-4 lists the additional requirements for the PCI Express 2x4 auxiliary power connector.

Table 8-4: Additional Requirements

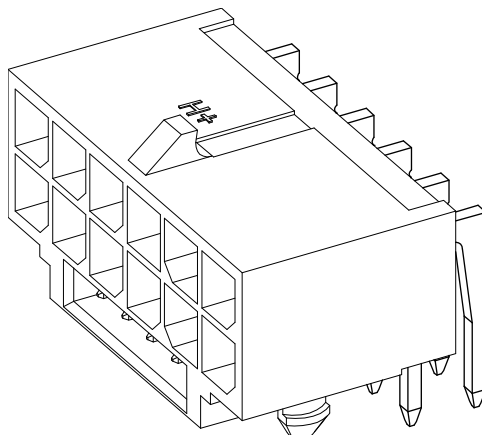
Parameter	Procedure	Requirement
Flammability	UL94V-1 minimum	Material certification or certificate of compliance required with each lot to satisfy the Underwriters Laboratories follow-up service requirements.
Lead-free soldering		Connector must be compatible with lead free soldering process.
Connector Color		Color of the connector is recommended to be black. Exceptions will be made for color coding schemes that call for a different color of this connector.

9. PCI Express 12VHPWR Auxiliary Power Connector Definition

This chapter defines the PCI Express 12VHPWR auxiliary power connector and cable assembly.

This connector design is introduced to support the 600 W card. The 12VHPWR connector will not mate with PCI Express 2x3 and 2x4 Auxiliary Power connectors. The 12VHPWR connector power pins have a 3.0 mm spacing, while the contacts in a 2x3 and 2x4 connector lie on a larger 4.2 mm pitch.

Figure 9-1 shows the un-mated 12VHPWR Add-in Card through-hole connector header. Twelve large contacts carry the power rail and four smaller contacts beneath carry sideband signals.



Dimension Tolerance, unless otherwise specified is: X.X = ± 0.25 mm, X.XX = ± 0.20 mm

Figure 9-1: 12VHPWR PCB Header

9.1. 12VHPWR Auxiliary Power Connector Performance Requirements

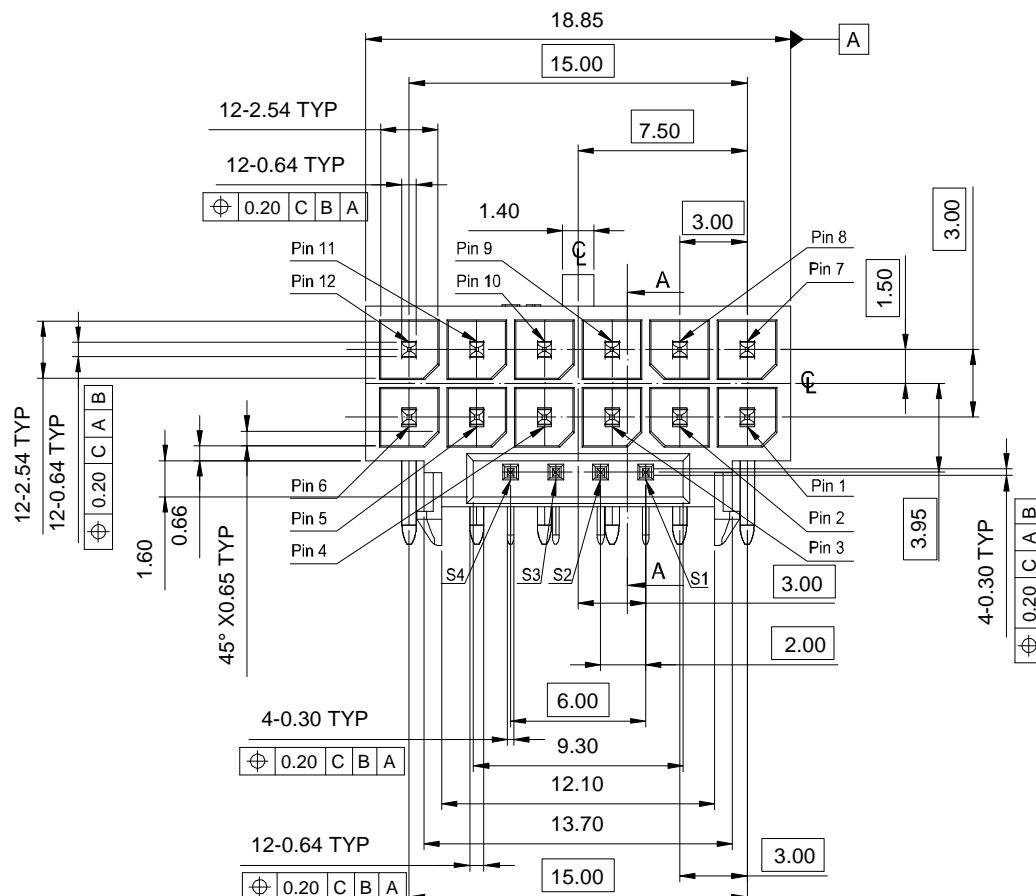
The 12VHPWR power connector delivers up to 55 A of continuous current to provide a maximum of 600 W of power to the Add-in Card on a 12 V Aux rail. Detailed voltage and current requirements for the 12V Aux rail are found in Table 4-2.

The connector performance requirements are as follows:

- Power Pin Current Rating: (Excluding sideband contacts) 9.2 A per pin/position with a limit of a 30 °C T-Rise above ambient temperature conditions at +12 V VDC with all twelve contacts energized. The connector body must display a label or embossed H+ character to indicate support of 9.2 A/pin or greater. See [Figure 1-1](#) for the approximate positioning of the marker on the 12VHPWR Right Angle (R/A) PCB Header.
- Mated Connector Latch Retention: 45.00 N minimum when plug pulled axially.

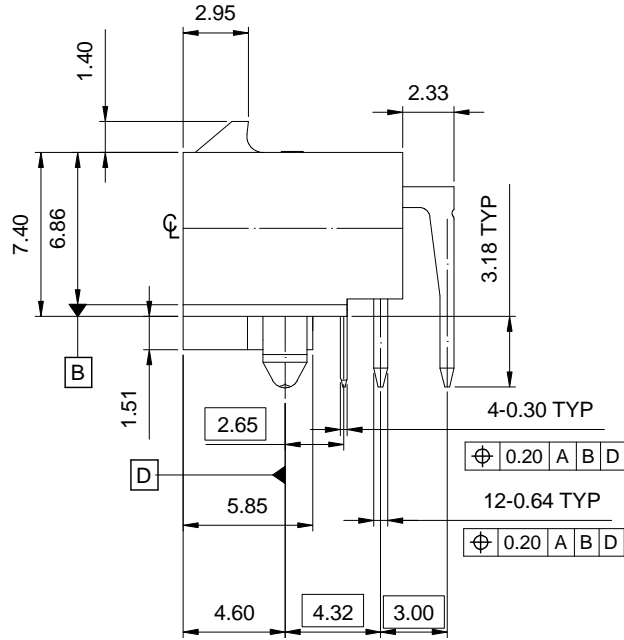
9.2. 12VHPWR Header

Figure 9-2 through Figure 9-5 show the dimensions and pinout for 12VHPWR PCB header.



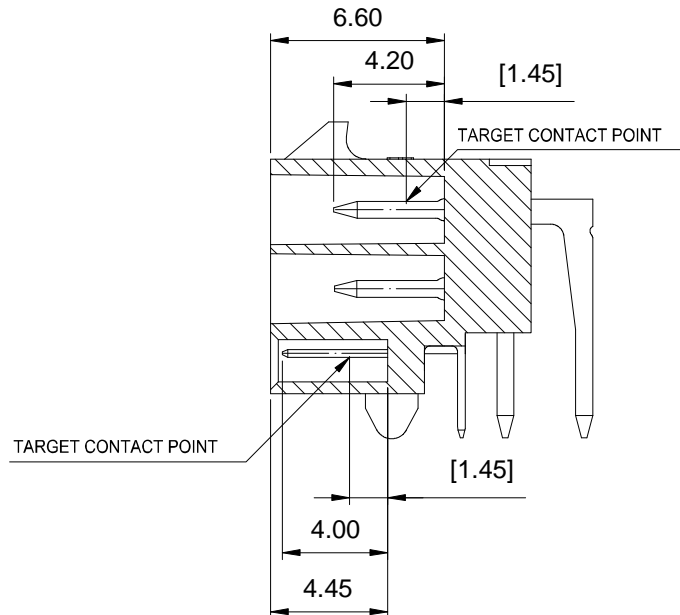
Dimension Tolerance, unless otherwise specified is: X.X = ± 0.25 mm, X.XX = ± 0.20 mm

Figure 9-2: 12VHPWR PCB Header



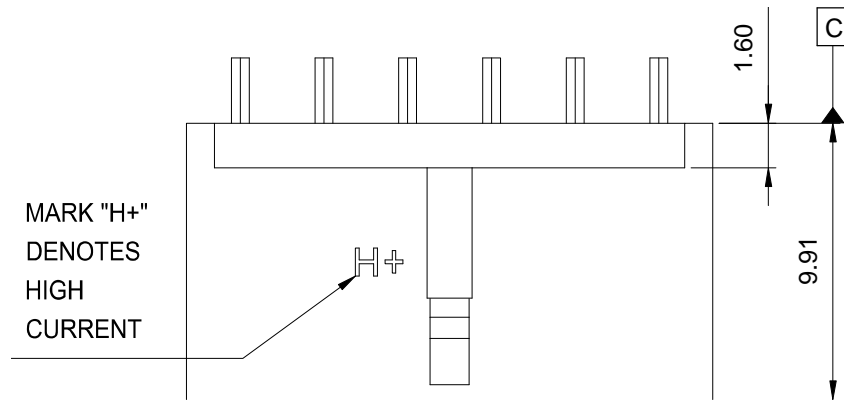
Dimension Tolerance, unless otherwise specified is: X.X = ± 0.25 mm, X.XX = ± 0.20 mm

Figure 9-3: 12VHPWR PCB Header, Side View



Dimension Tolerance, unless otherwise specified is: X.X = ± 0.25 mm, X.XX = ± 0.20 mm

Figure 9-4: 12VHPWR PCB Header, Side View, Highlighting Contact Dimensions



Dimension Tolerance, unless otherwise specified is: X.X = ± 0.25 mm, X.XX = ± 0.20 mm

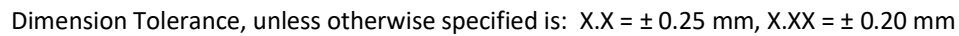
Figure 9-5: 12VHPWR PCB Header, Top View

9.2.1. 12VHPWR Header Construction

- Housing Material: Thermoplastic Glass Fiber Filled, UL94V-0
- Color: Black
- Pin Contact Material: Copper Alloy
- Power Pin Contact Plating: Tin plated on contact area
- Signal Pin Contact Plating: Tin plated on contact area
- All dimensions are in mm
- Connector must be compatible with lead-free soldering process
- Connector mechanical Keying: See Figure 9-2

9.2.2. PCB Footprint

Figure 9-6 shows the recommended PCB footprint for the 12VHPWR Right Angle Header. All dimensions are in mm. All six header power and ground pins must be joined to the same PCB plane within the connector pinfield on the Add-in Card.



This diagram illustrates the exploded view of a 10GBase-T RJ45 connector assembly. It shows the following components from top to bottom:

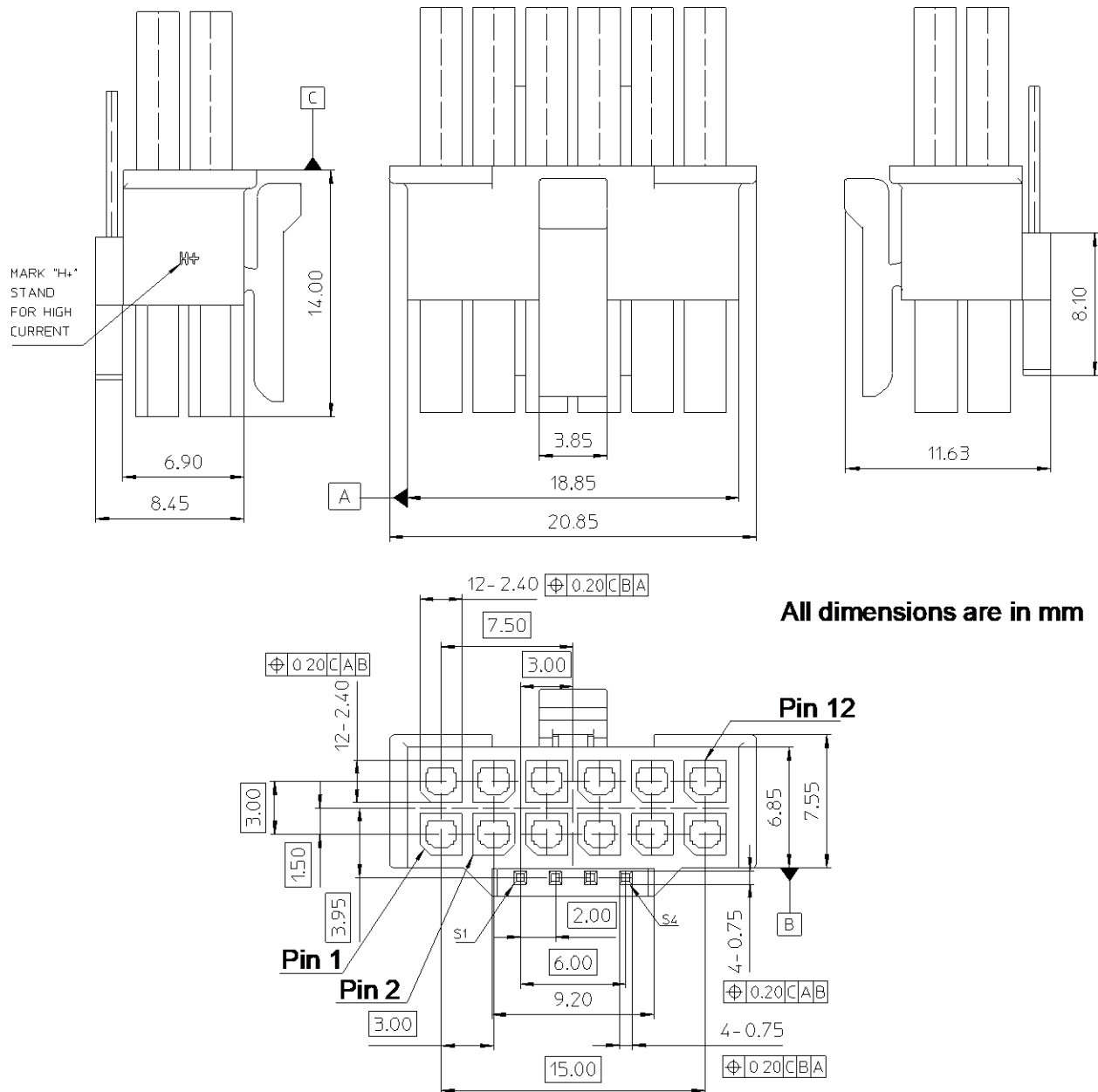
- Shielding Shell:** A large, U-shaped metal component designed to protect the internal contacts from electromagnetic interference (EMI).
- Connector Housing:** A plastic component that houses the internal contacts and provides a mounting point for the shielding shell.
- Contacts:** A series of metal pins (contacts) that are inserted into the housing. These contacts are responsible for establishing the electrical connection with the network cable.
- Network Cable:** A standard Ethernet cable with a braided shield and four twisted pairs of conductors, which are shown being inserted into the contacts.

Figure 9-7: 12VHPWR Cable Plug Connector

9.3.1. Cable Assembly

Figure 9-8 shows the cable plug connector housing for the 12VHPWR connector. All dimensions are in mm.

The 12VHPWR cable must be capable of carrying 55 A of continuous current (9.2 A/wire) to provide a maximum of 600 W of power.



Dimension Tolerance, unless otherwise specified is: X.X ± 0.25 mm, X.XX ± 0.20 mm

Figure 9-8: 12VHPWR Cable Plug Connector Assembly

Dimension Tolerance, unless otherwise specified is: X.X ± 0.25 mm, X.XX ± 0.20 mm

9.3.1.1 12VHPWR Cable Plug Housing Assembly and Contact Construction

- Housing Material: Thermoplastic Glass Fiber Filled, UL94V-0
- Color: Black
- Pin Contact Material: Copper Alloy
- Power Pin Contact Plating: Tin plated on contact area
- Signal Pin Contact Plating: Tin plated on contact area
- All dimensions are in mm
- Connector must be compatible with lead-free soldering process.

Wire Details:

- Power/Ground Pin Wire Size: 16 AWG (All 12 pins must be connected to the power supply using 16 AWG cable)
- Signal Pin Wire Size: 28 AWG

9.3.1.2 12VHPWR Auxiliary Power Connector System Pin Assignment

See Table 9-1 for a list of the 12VHPWR pin assignments. The electrical function for the sideband pins S1- S4 are detailed in Section 5.3.

Table 9-1: 12VHPWR Cable Plug Pin Assignment

Pin	Signal
1 to 6	+12 V
7 to 12	Ground
S1	CARD_PWR_STABLE
S2	CARD_CBL_PRES#
S3	SENSE0
S4	Do not use. Reserved for future use.

10. PCI Express 48VHPWR Auxiliary Power Connector Definition

This chapter defines the PCI Express 48VHPWR auxiliary power connector and cable assembly.

Figure 10-1 shows the un-mated 48VHPWR board side connector and cable connector. The two large contacts carry the power rail and the four smaller contacts underneath carry sideband signals.

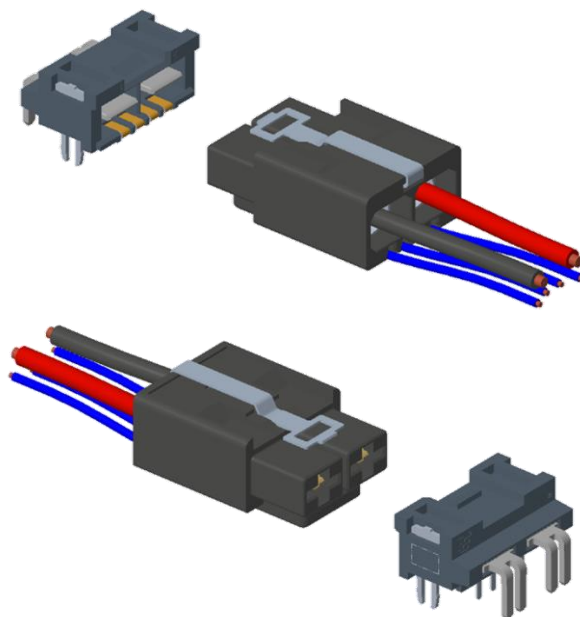


Figure 10-1. 48VHPWR Plug Mating with a 48HVPWR Header

10.1. 48VHPWR Auxiliary Power Connector Performance Requirements

The 48VHPWR power connector delivers up to 15 A of continuous current to provide a maximum of 600 W of power to the Add-in Card on a 48 V Aux rail. Detailed voltage and current requirements for the +48 V rail are found in Table 4-2.

The 48VHPWR power connector performance requirements are as follows:

- Power Pin Current Rating: 15.0 A per pin/position maximum to a 30°C T-Rise above ambient temperature conditions at +48 VDC with both power contacts energized
- Mated Connector Retention: 100.00 N minimum when plug pulled axially



IMPLEMENTATION NOTE

48VHPWR Auxiliary Power Connector Current Rating

System integrators should ensure that the power contacts used in the 48VHPWR connector are of the correct rating to meet the 15 A requirement. Appropriate derating and clearances should be used.

10.2. 48VHPWR Header

10.2.1. Connector Drawing

Figure 10-2 shows the details of a 48VHPWR, right-angle (R/A) through-hole header.

10.2.1.1 48VHPWR Header

- Housing Color: Black
- Housing Material: LCP
- Pin Contact and Latch Base Material: Copper Alloy
- Power Pin Contact Plating: 3 μ m Silver over Nickel Plated
- Signal Pin Contact Plating: 0.4 μ m Gold over Nickel Plated
- Latch Plating: Sn Plated
- All dimensions are in mm

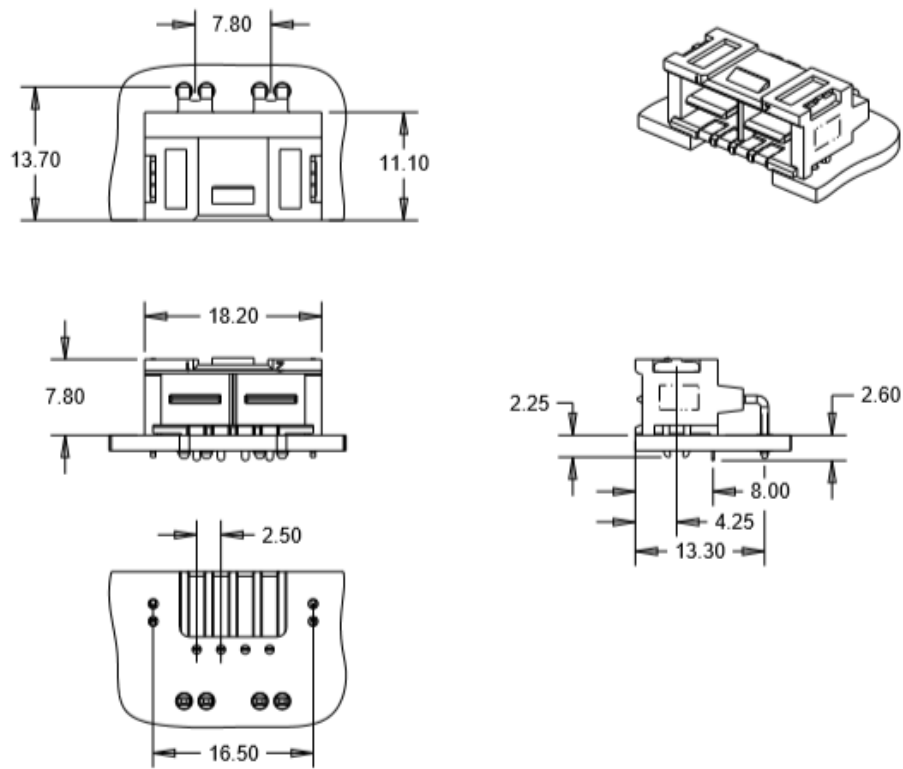


Figure 10-2. 48VHPWR Right Angle Through-Hole Header Drawing

10.2.2. PCB Footprint

Figure 10-3 shows the recommended PCB footprint for the 48VHPWR Right Angle through-hole header. All dimensions are in mm.

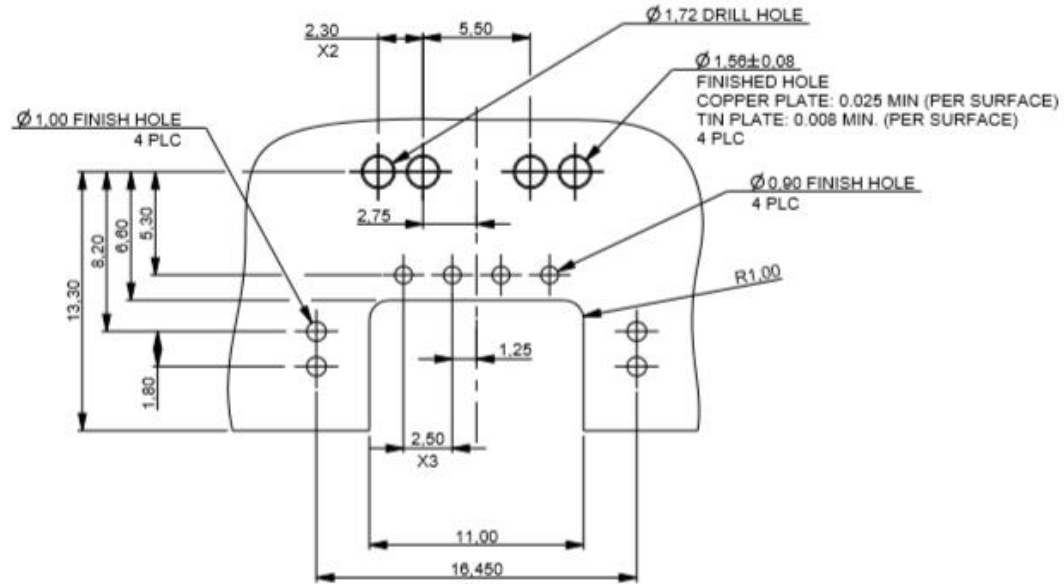


Figure 10-3. 48VHPWR Right Angle Through-Hole Header Recommended PCB Footprint

10.3. 48VHPWR Cable Assembly and Header

Figure 10-4 shows the cable plug housing for the 48VHPWR connector.

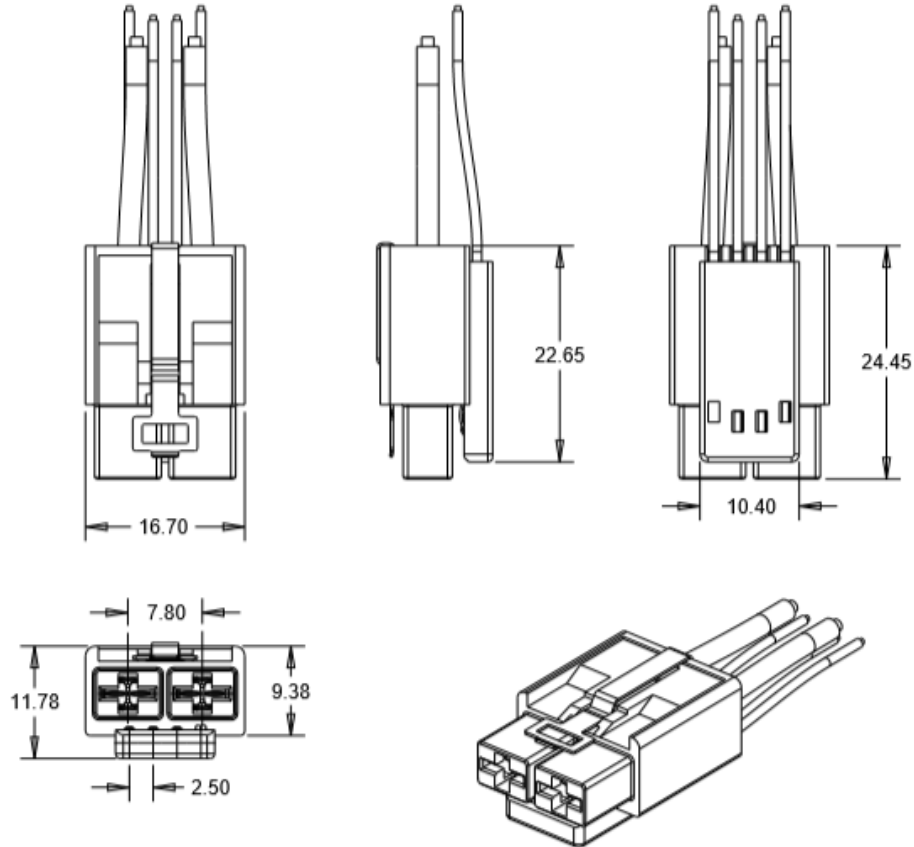


Figure 10-4. 48VHPWR Cable Plug Connector Housing

Cable Assembly Contact and Housing Details:

- Housing Color: Black
- Housing Material: LCP
- Pin Contact and Latch Base Material: Copper Alloy
- Power Pin Contact Plating: 3 μm Silver over Nickel Plated
- Signal Pin Contact Plating: 0.4 μm Gold over Nickel Plated
- Latch Plating: Sn Plated
- All dimensions are in mm.

Wire Details:

- Power/Ground Pin Wire Size: 16 AWG
- Signal Pin Wire Size: 22 AWG

10.3.1. 48VHPWR Connector

Figure 10-5 shows the location to press the latch and release the locking mechanism, allowing connector de-mating.

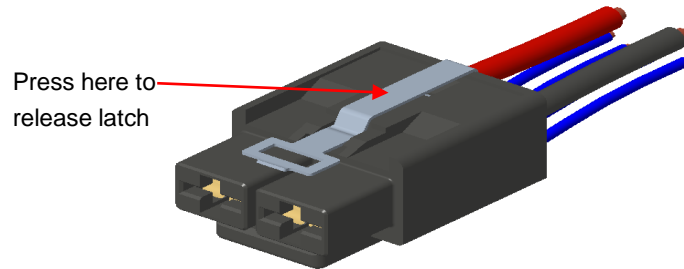


Figure 10-5. 48VHPWR Connector Latch Release

10.4. 48VHPWR Auxiliary Power Connector System Pin Assignment

Figure 10-6 and Figure 10-7 show the pinout for the 48VHPWR auxiliary power connector. Table 10-1 shows the 12VHPWR pin assignments and Table 10-2 lists additional connector requirements.

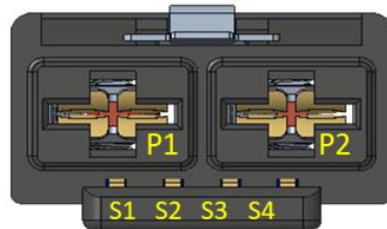


Figure 10-6. 48VHPWR Auxiliary Power Connector Pinout, Plug Side

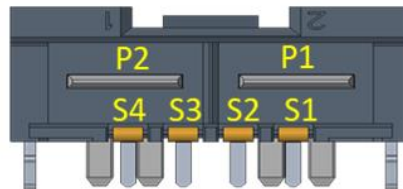


Figure 10-7. 48VHPWR Auxiliary Power Connector Pinout, Header Side

See Table 10-1 for a list of the 48VHPWR pin assignments. The electrical functions for the sideband pins S1-S4 are detailed in Section 5.3.

Table 10-1: 48VHPWR Auxiliary Power Connector Pin Assignment

Pin	Signal
P1	+48 V
P2	Ground
S1	CARD_PWR_STABLE
S2	CARD_CBL_PRES#
S3	SENSE0
S4	SENSE1

Table 10-2 lists additional connector requirements.

Table 10-2: Additional Requirements

Parameter	Procedure	Requirement
Flammability	UL94V-0	Material certification or certificate of compliance required with each lot to satisfy the Underwriters Laboratories follow-up service requirements.
Lead-free Soldering		Connector must be compatible with lead free soldering process.
Connector Color		Color of the connector is recommended to be black. Exceptions will be made for color coding schemes that call for a different color of this connector.

11. Add-in Card Form Factors and Implementation

11.1. Add-in Card Form Factors

To enable the reuse of existing chassis slots, the PCI Express Add-in Cards are similar to the PCI Add-in Card form factor. Two PCI Express Add-in Card heights are defined: standard height and low profile. The card height is measured from the bottom of the edge-finger tab to the top of the card (see Figure 11-1B and Figure 11-3). Table 11-1 lists the Add-in Card sizes.

Table 11-1: Add-in Card Sizes

Add-in Card	Height	Length
Standard height	111.28 mm (4.381 inches) maximum	See Figure 11-1B
Low profile	68.09 mm (2.718 inches) maximum	See Figure 11-8

A PCI Express DUAL-SLOT Add-in Card and TRIPLE-SLOT Add-in Card have the same dimensions as a standard height full length card, except there is component side height increase. See Figure 11-11 and Figure 11-12. The maximum length specifies what the system design must accommodate. An Add-in Card can be any length up to the maximum for a length interval. For example, a standard height card with a 177.80 mm (7.00 inches) length can be installed in a system that accommodates 241.30 mm (9.5 inches) maximum length cards, but a system that only accommodates 167.65 mm (6.6 inches) maximum length cards will not support this card.



IMPLEMENTATION NOTE

PCI Express Card Length

Not all system designs will support 312 mm (12.3 inches) full-length cards. It is strongly recommended that PCI Express Add-in Cards be designed with a 241.30 mm (9.5 inches) maximum length. This applies to SINGLE-SLOT, DUAL-SLOT, and TRIPLE-SLOT Add-in Card designs.

Figure 11-1B and Figure 11-3 show the standard PCI Express card form factor without and with the I/O bracket, respectively.

The following notes apply to Figure 11-1B through Figure 11-3:

- The mounting holes illustrated in Figure 11-1B are required only on the right end of the full-length card 312.00 mm (12.3 inches). Those holes may be needed to install an optional PCI Add-in Card retainer.
- The mounting holes and keepout zones around them marked as note 3 in Figure 11-1B may be used on those cards in which the I/O bracket is mounted to the card directly and are for reference purposes only. The purpose of this keepout is to ensure that the card cannot short out on the I/O bracket. Add-in Card providers must ensure that their card cannot short out the I/O bracket. On full-length cards, a keepout of 5.08 mm (0.2 inches) is required to prevent card components from being damaged by the system's card guides (see Figure 11-1B).
- Retention requirements are defined in Section 6.2.
- Special attention shall be given to high mass Add-in Cards. This specification defines the additional feature and keepouts for high-mass cards for card retention shown in Figure 11-3, A and B. This retention feature is not limited to higher-mass cards and may be used by any card.

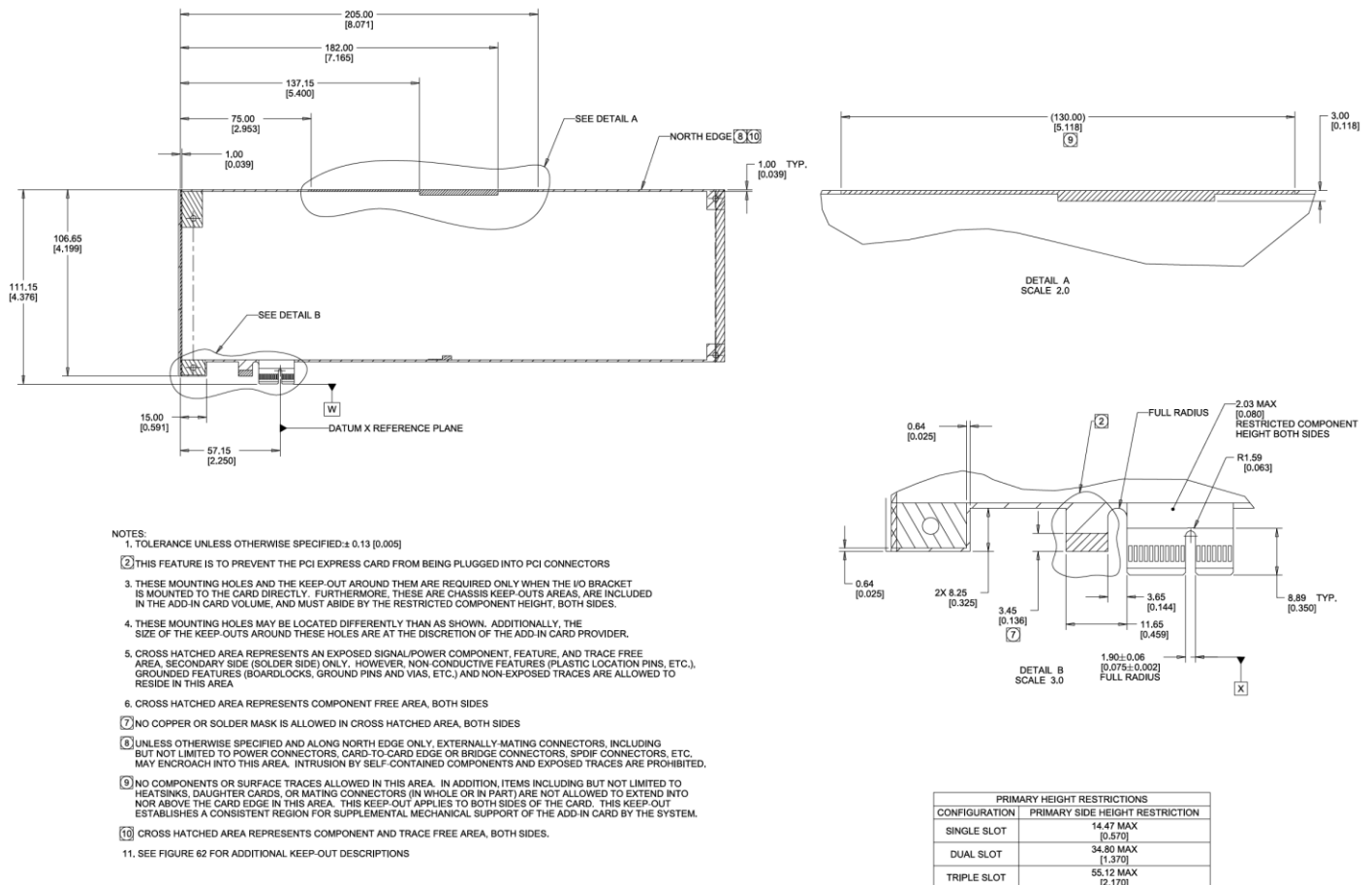


Figure 11-1A: Standard Height PCI Express Add-in Card without the I/O Bracket

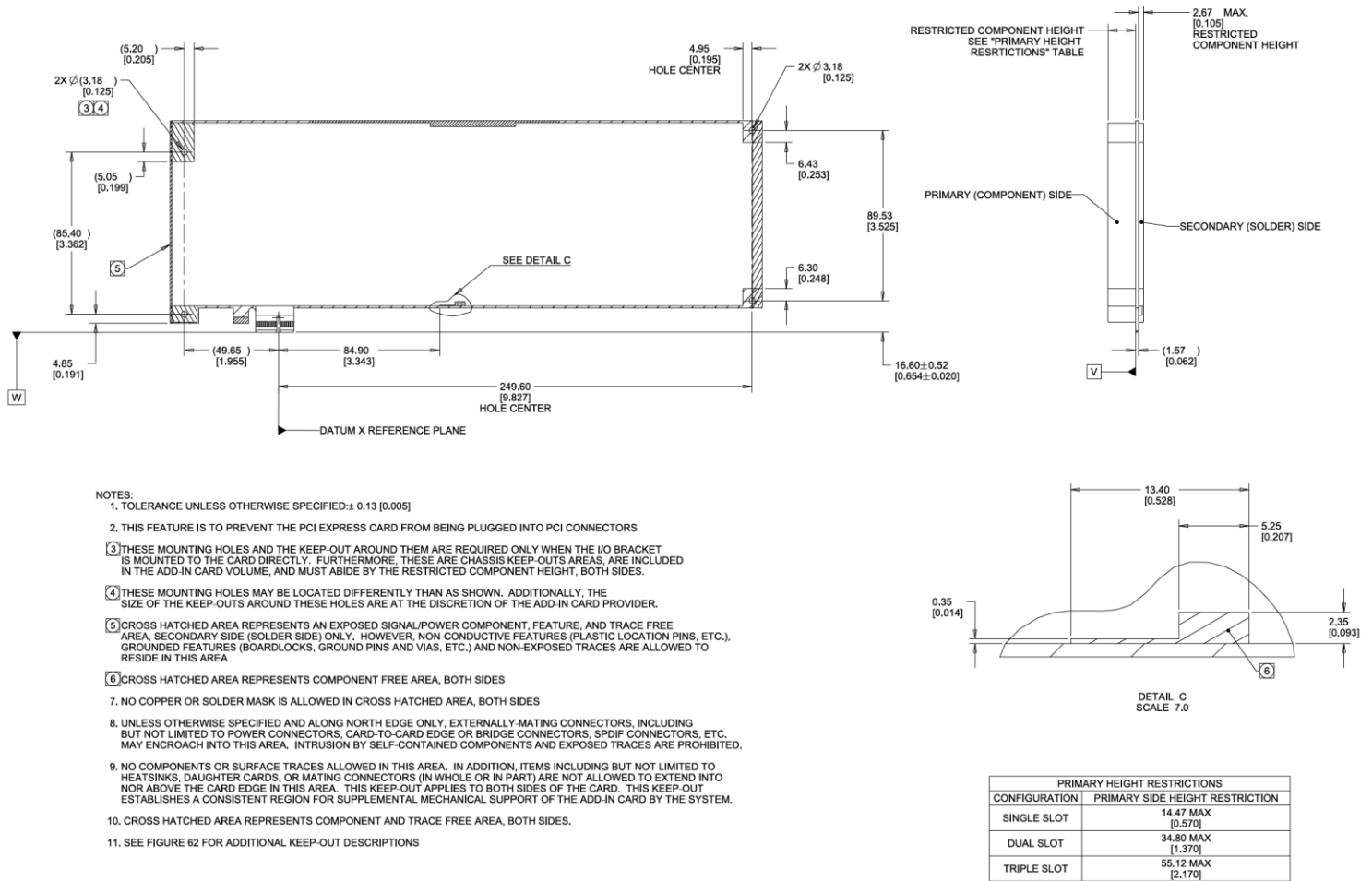
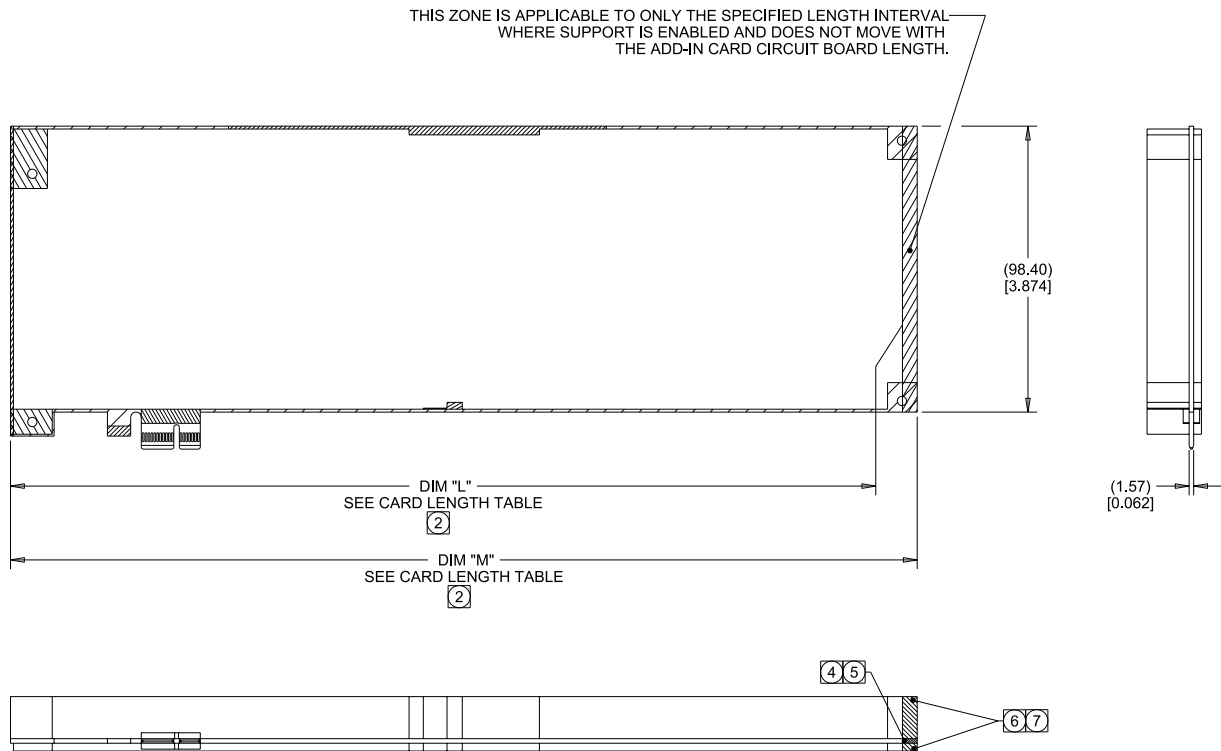


Figure 11-1B: Standard Height PCI Express Add-in Card without the I/O Bracket



NOTES:

1. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.13 [0.005]
- (2) DIMENSIONS ESTABLISH A CONSISTENT VOLUME FOR END CARD MECHANICAL SUPPORT
3. FOR EACH LENGTH INTERVAL, DIMENSION "M" ALSO DESCRIBES THE MAXIMUM OVERALL LENGTH OF THE ADD-IN CARD ASSEMBLY
- (4) FOR EACH SPECIFIED LENGTH INTERVAL WHERE OPTIONAL SUPPORT IS ENABLED, FEATURES OF THE ADD-IN CARD ASSEMBLY (PCB OR SHEET METAL) MUST INTERSECT WITH THIS VOLUME. IF PART OF THE ADD-IN CARD CIRCUIT BOARD OCCUPIES THIS VOLUME, THIS MUST BE A COMPONENT AND SURFACE TRACE FREE AREA, ON BOTH SIDES OF THE PCB.
- (5) FOR EACH SPECIFIED LENGTH INTERVAL WHERE OPTIONAL SUPPORT IS ENABLED, SYSTEMS MUST ACCOMMODATE THE ENTIRE DESCRIBED VOLUME. OTHERWISE, ISSUES INCLUDING BUT NOT LIMITED TO NON-RETENTION OF ADD-IN CARD, FIT INTERFERENCE, ETC. COULD OCCUR.
- (6) FOR THE FULL-LENGTH INTERVAL, IT IS REQUIRED THAT ADD-IN CARD ITEMS INCLUDING BUT NOT LIMITED TO HEATSINKS, DAUGHTER CARDS, OR MATING CONNECTORS (IN WHOLE OR IN PART) ARE NOT ALLOWED TO EXTEND INTO THIS VOLUME
- (7) FOR THE HALF-LENGTH AND THREE QUARTER LENGTH INTERVAL, IF OPTIONAL SUPPORT IS ENABLED, IT IS REQUIRED THAT ADD-IN CARD ITEMS INCLUDING BUT NOT LIMITED TO HEATSINKS, DAUGHTER CARDS, OR MATING CONNECTORS (IN WHOLE OR IN PART) ARE NOT ALLOWED TO EXTEND INTO THIS VOLUME.

CARD LENGTH TABLE		
LENGTH INTERVAL	DIM "L"	DIM "M"
HALF LENGTH	162.57 [6.400]	167.65 MAX [6.600]
THREE-QUARTER LENGTH	248.92 [9.800]	254.00 MAX [10.000]
FULL LENGTH	306.92 [12.083]	312.00 MAX [12.283]

Figure 11-2: Chassis Interface Zones on Right/East Edge of Add-in Card

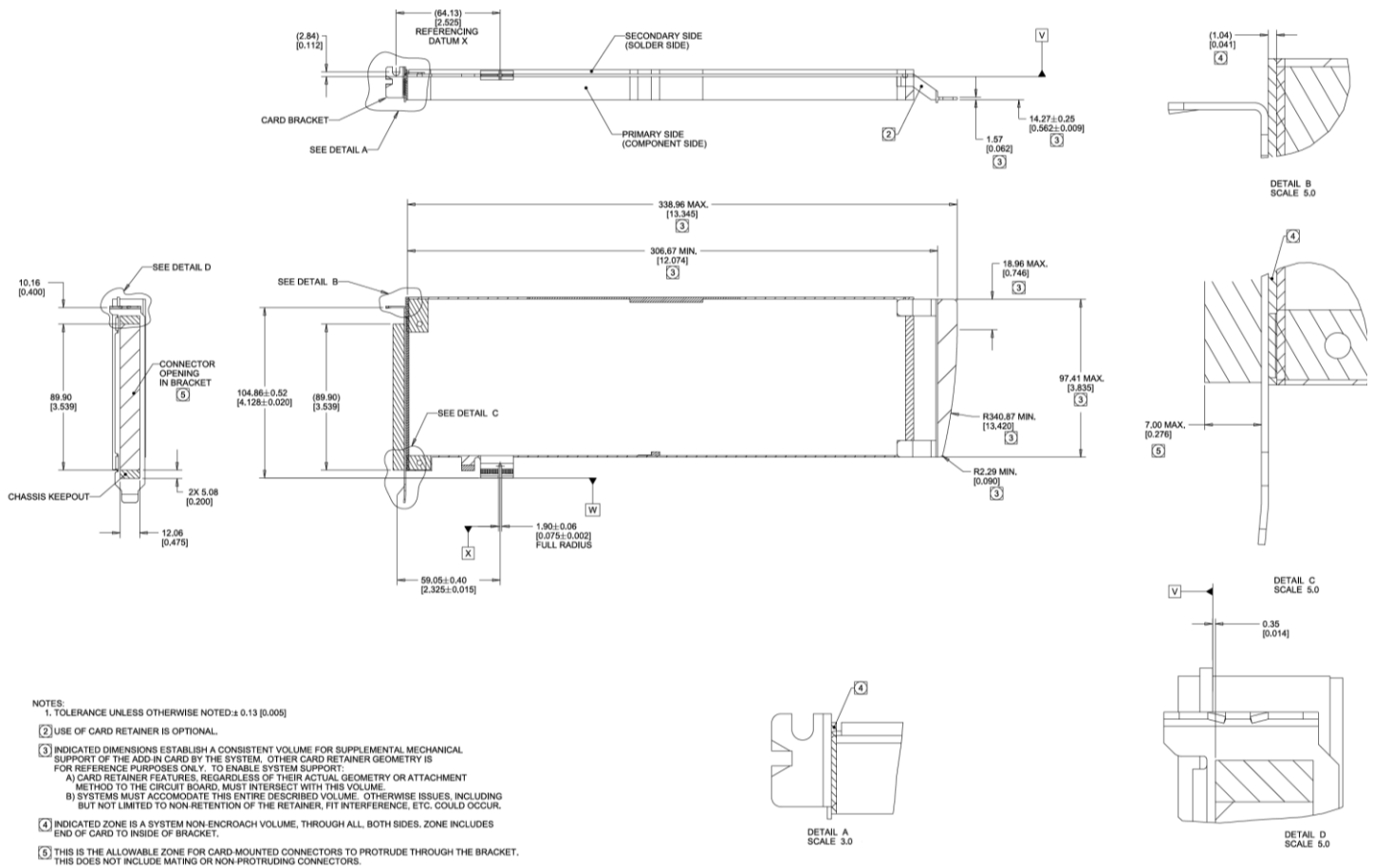


Figure 11-3: Standard Height PCI Express Add-in Card with the I/O Bracket and Card Retainer

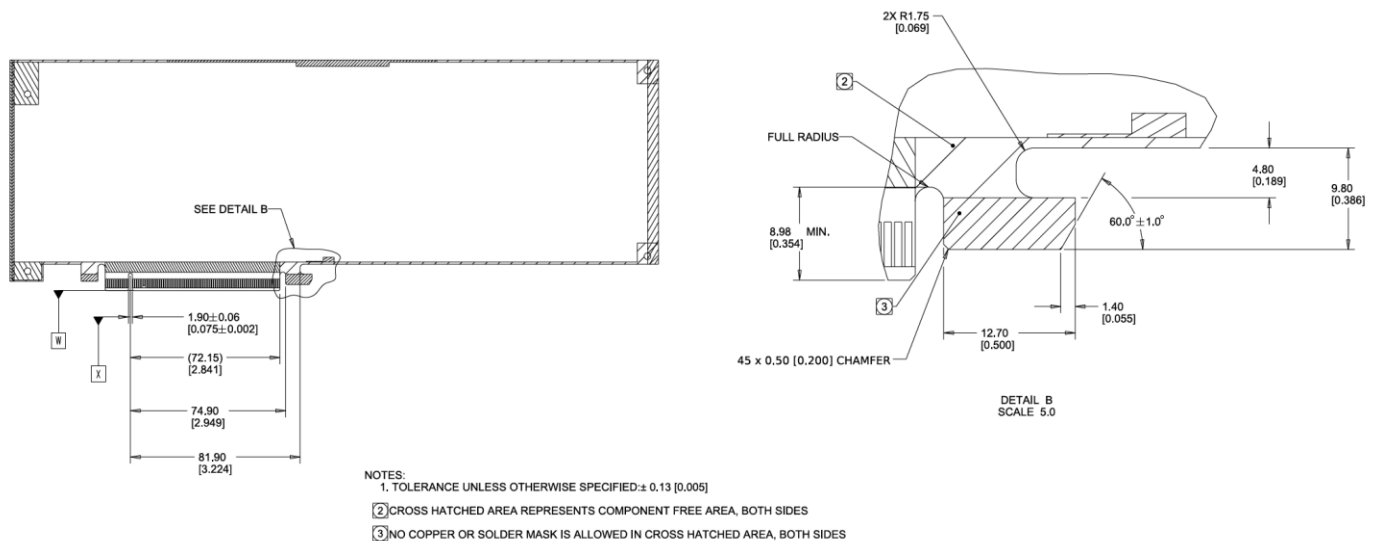


Figure 11-4: Additional Feature and Keepouts for a High Mass Card

The 3.0 mm keepout on the top of the card is to accommodate system or chassis-level card retention solutions at each OEM's discretion. To facilitate a chassis level retention solution, the height of the standard height Add-in Card is required to be fixed: 111.15 mm \pm 0.13 mm. The "hockey stick" shaped feature and keepout defined on the bottom of the card is to allow retention mechanisms either mounted directly on the system board or integrated into the connector. If present, the position (relative to Datum X in Figure 11-4) of the "hockey stick" must remain the same, regardless of the length of the connector/edge-fingers. This feature and keepout are also required for any low-profile card that is required to be retention ready.

All retention mechanisms that are intended for high mass cards must use the feature/keepout defined in Figure 11-4. However, the specific retention mechanism design is left to the system manufacturers' choice. Figure 11-5 shows the standard PCI Express I/O bracket, which is the same as the PCI bracket. The mounting tabs of the bracket shown in Figure 11-5 are to be mounted onto the secondary side of the card, as illustrated in Figure 11-3. However, a user also has the option to have a bracket with the mounting tabs mounted onto the primary side of the card. Exact locations of contact between the bracket and the Add-in Card PCB (and the associated keepout zones) are at the discretion of the Add-in Card provider and must not be assumed to be fixed by the system integrator for additional card retention. Any dimensions in figures which describe geometry for "PCB attach" are REFERENCE.

The detailed Add-in Card edge-finger dimensions are defined in Section 6.2, which describes the connector mating interface. The edge-finger portions of the PCI Express cards are required to have bevels or chamfers as defined in Figure 6-5.

Figure 11-6 A and B, and Figure 11-8 show, respectively, the low-profile PCI Express Add-in Card form factor without and with the bracket, while Figure 11-9 shows the low-profile Add-in Card I/O bracket. When mounting a low-profile card into a full height PCI slot, the standard I/O bracket must be modified to add a stiffening flange. Figure 11-10 shows the modified full height I/O bracket for low profile cards.

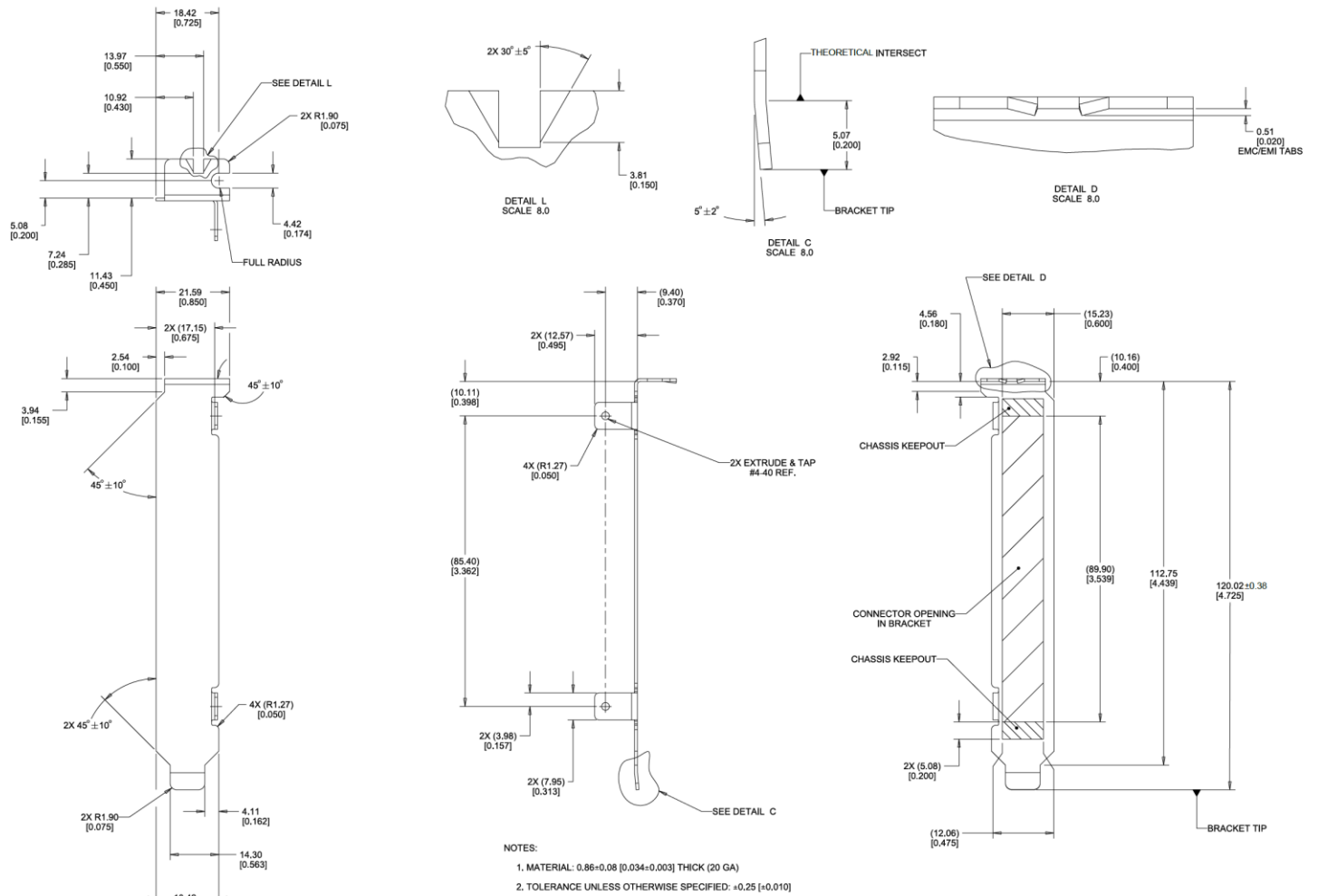


Figure 11-5: Standard Add-in Card I/O Bracket

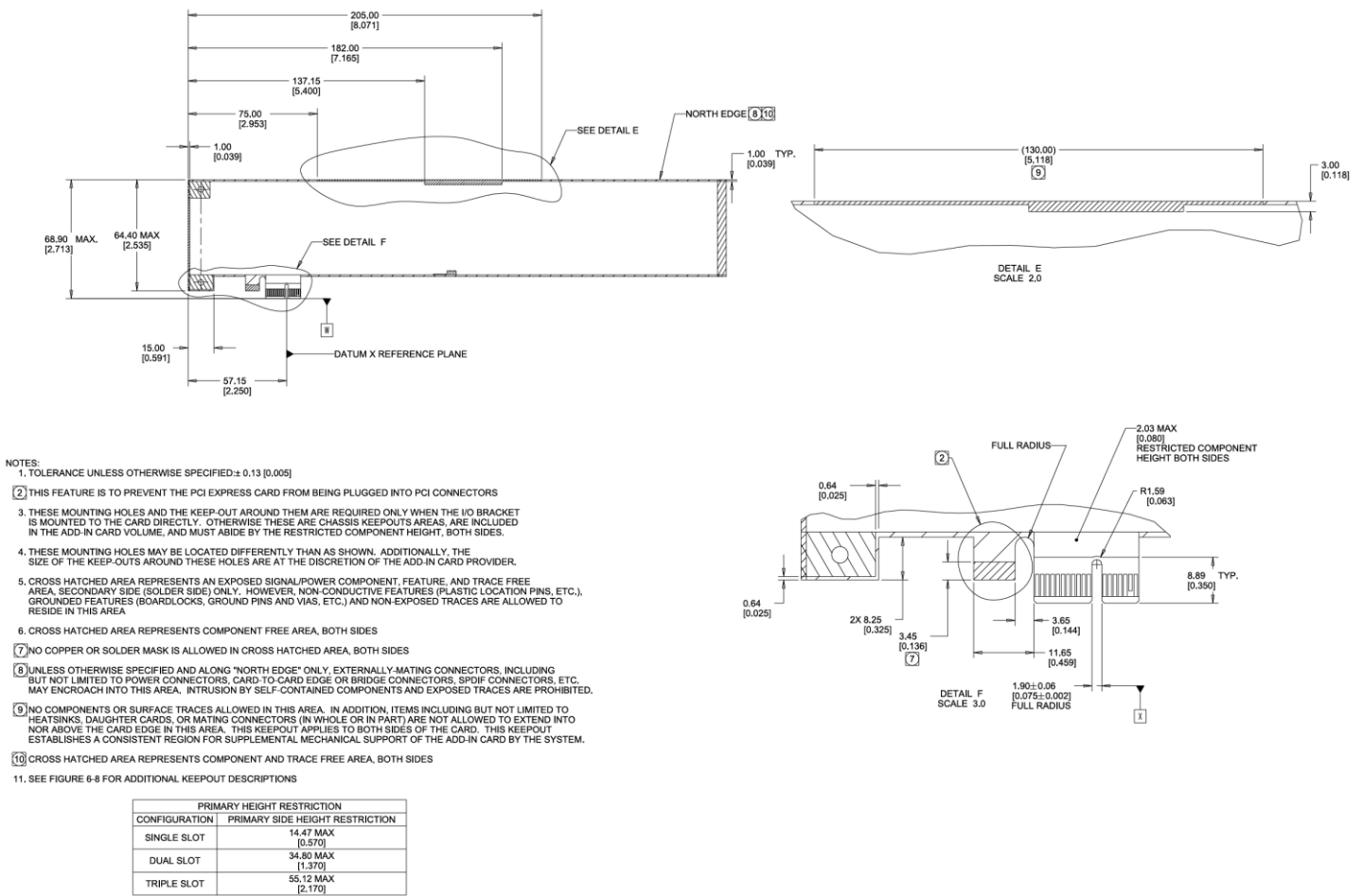
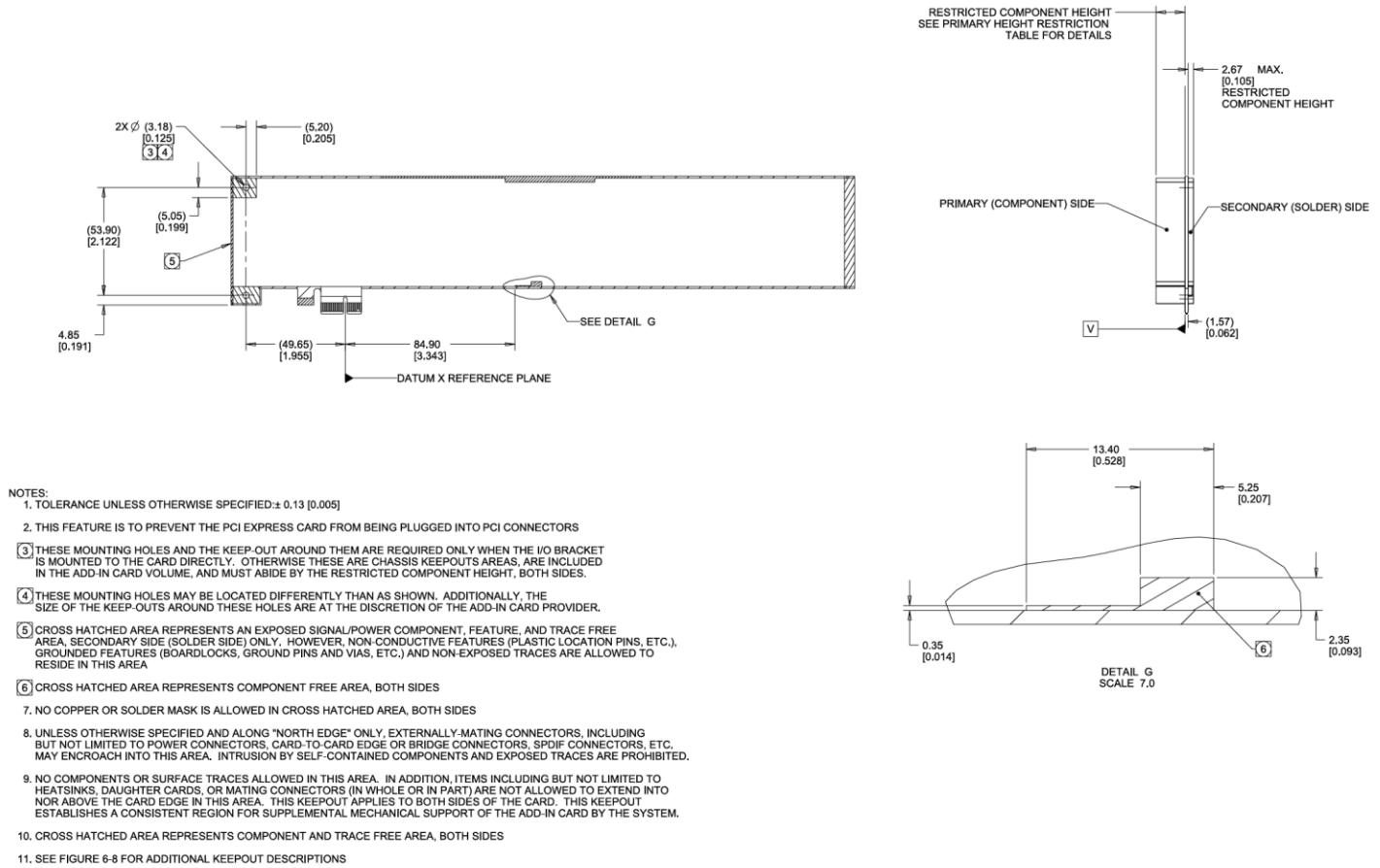
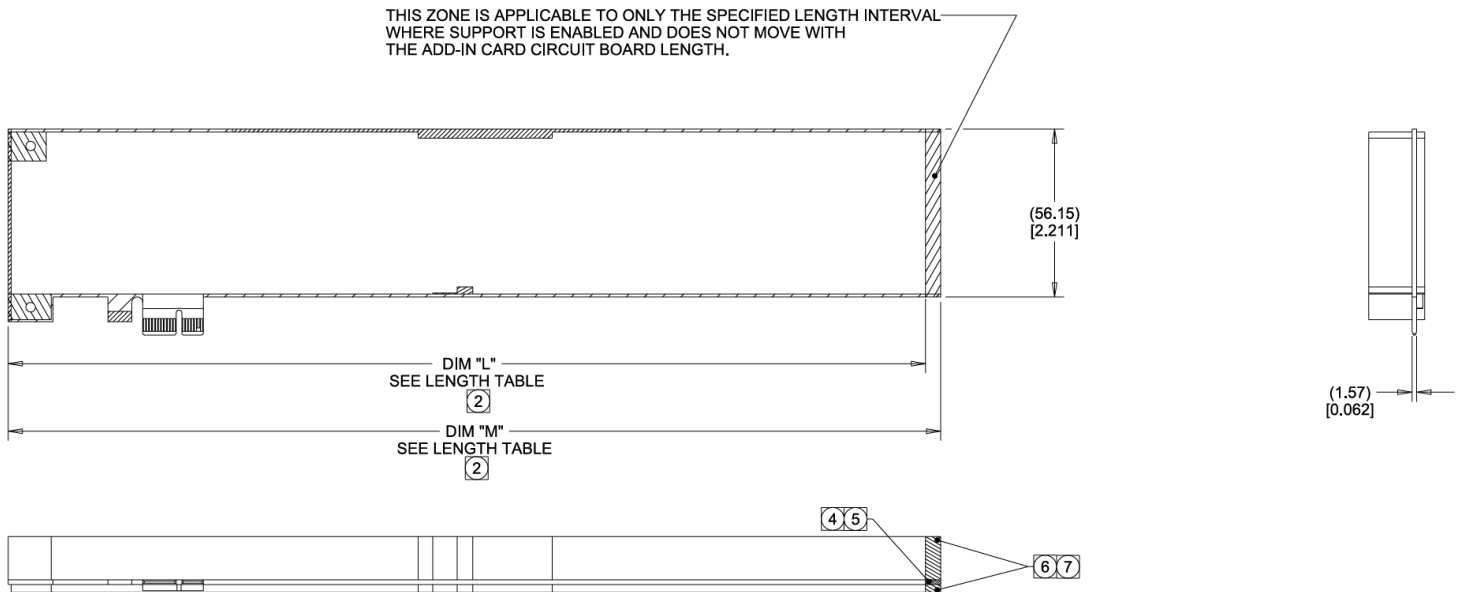


Figure 11-6A: Low Profile PCI Express Add-in Card without the I/O Bracket



PRIMARY HEIGHT RESTRICTION	
CONFIGURATION	PRIMARY SIDE HEIGHT RESTRICTION
SINGLE SLOT	14.47 MAX [0.570]
DUAL SLOT	34.80 MAX [1.370]
TRIPLE SLOT	55.12 MAX [2.170]

Figure 11-6B: Low Profile PCI Express Add-in Card without the I/O Bracket



NOTES:

1. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.13 [0.005]
2. DIMENSIONS ESTABLISH A CONSISTENT VOLUME FOR END CARD MECHANICAL SUPPORT
3. FOR EACH LENGTH INTERVAL, DIMENSION "M" ALSO DESCRIBES THE MAXIMUM OVERALL LENGTH OF THE ADD-IN CARD ASSEMBLY
4. FOR EACH SPECIFIED LENGTH INTERVAL WHERE OPTIONAL SUPPORT IS ENABLED, FEATURES OF THE ADD-IN CARD ASSEMBLY MUST INTERSECT WITH THIS VOLUME. IF PART OF THE ADD-IN CARD CIRCUIT BOARD, THIS MUST BE A COMPONENT AND SURFACE TRACE FREE AREA, BOTH SIDES.
5. FOR EACH SPECIFIED LENGTH INTERVAL WHERE OPTIONAL SUPPORT IS ENABLED, SYSTEMS MUST ACCOMMODATE THE ENTIRE DESCRIBED VOLUME. OTHERWISE, ISSUES INCLUDING BUT NOT LIMITED TO NON-RETENTION OF ADD-IN CARD, FIT INTERFERENCE, ETC. COULD OCCUR.
6. FOR THE FULL-LENGTH INTERVAL, IT IS REQUIRED THAT ADD-IN CARD ITEMS INCLUDING BUT NOT LIMITED TO HEATSINKS, DAUGHTER CARDS, OR MATING CONNECTORS (IN WHOLE OR IN PART) ARE NOT ALLOWED TO EXTEND INTO THIS VOLUME
7. FOR THE HALF-LENGTH AND THREE QUARTER LENGTH INTERVAL, IF OPTIONAL SUPPORT IS ENABLED, IT IS REQUIRED THAT ADD-IN CARD ITEMS INCLUDING BUT NOT LIMITED TO HEATSINKS, DAUGHTER CARDS, OR MATING CONNECTORS (IN WHOLE OR IN PART) ARE NOT ALLOWED TO EXTEND INTO THIS VOLUME.

LENGTH TABLE		
LENGTH INTERVAL	DIM "L"	DIM "M"
HALF LENGTH	166.65 [6.561]	167.65 MAX [6.600]
THREE-QUARTER LENGTH	248.92 [9.800]	254.00 MAX [10.000]
FULL LENGTH	306.92 [12.083]	312.00 MAX [12.283]

Figure 11-7: Chassis Interface Zone on Right/East Edge of Low-Profile Add-in Card

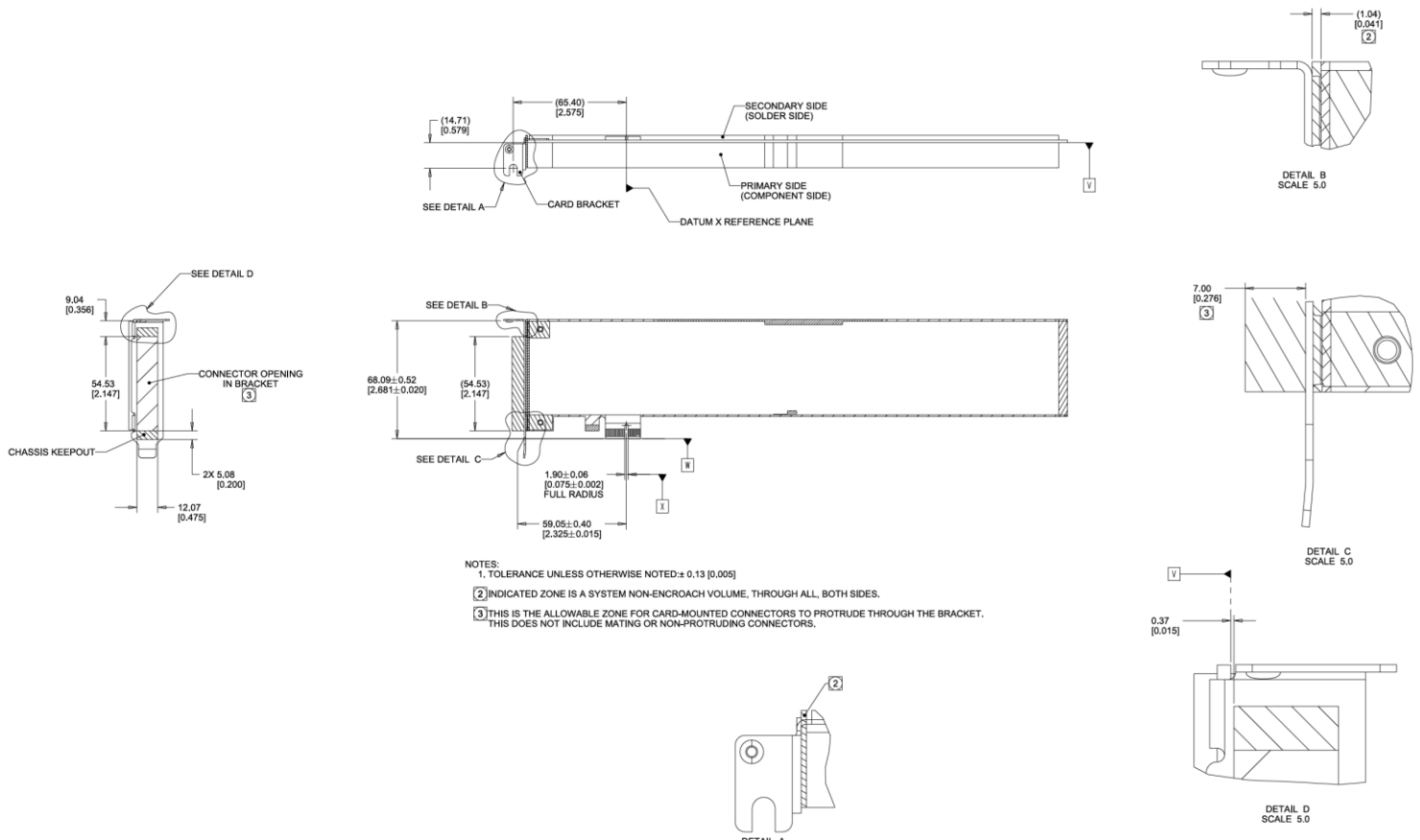
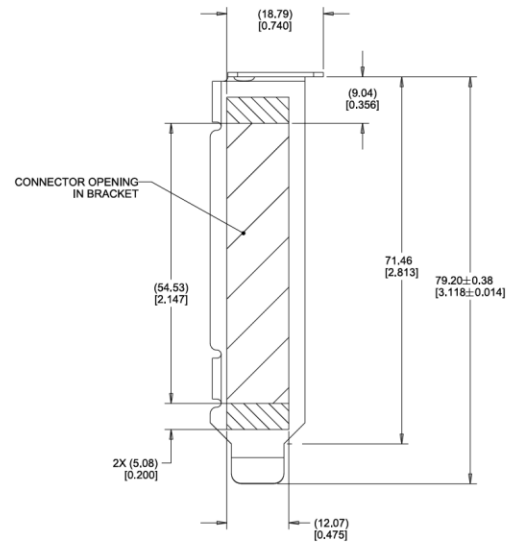
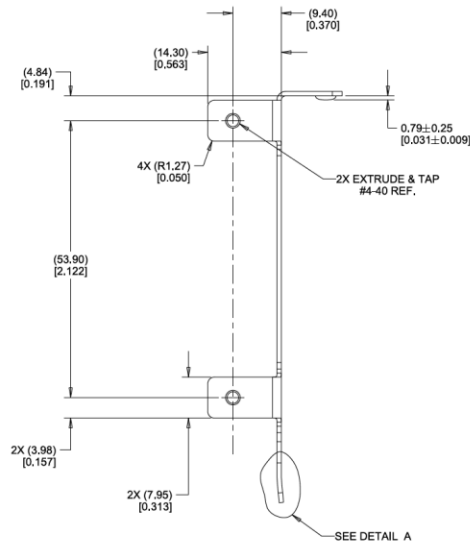
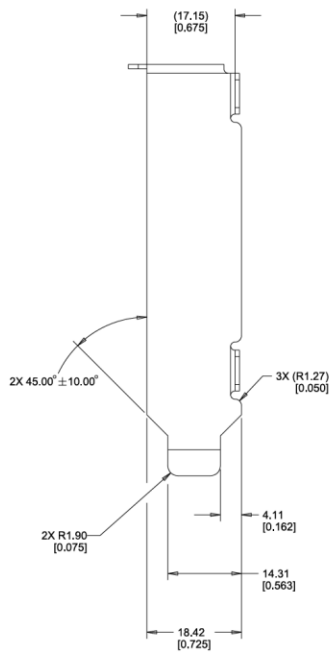
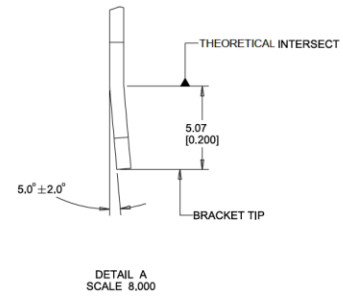
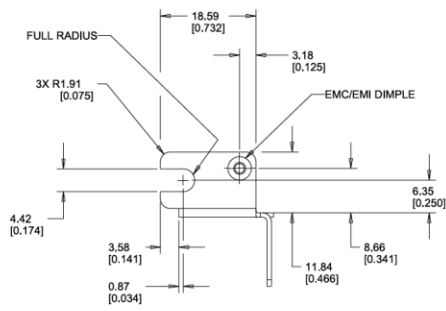


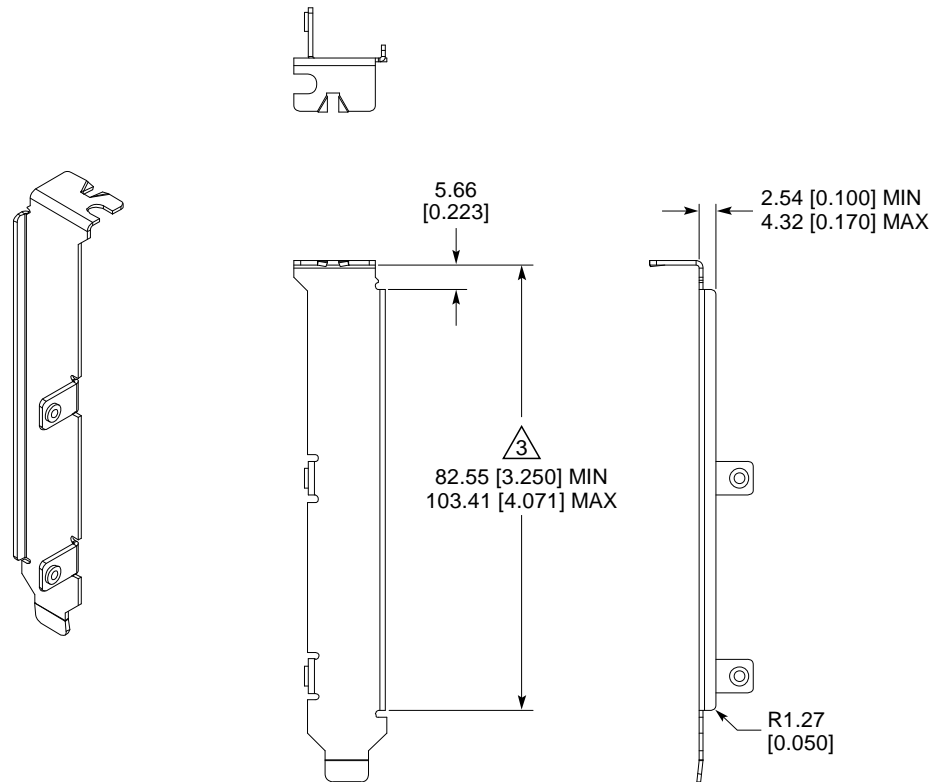
Figure 11-8: Low Profile PCI Express Add-in Card with the I/O Bracket



NOTES:

1. MATERIAL: 0.86±0.08 [0.034±0.003] THICK (20 GA)
2. TOLERANCE OTHERWISE SPECIFIED: ±0.25 [±0.010]

Figure 11-9: Low Profile I/O Bracket



NOTES:

1. STIFFENING FLANGE IS REQUIRED WHEN MOUNTING A LOW PROFILE CARD TO A FULL HEIGHT BRACKET.
2. STIFFENING FLANGE IS OPTIONAL WHEN MOUNTING A FULL HEIGHT CARD.

3 THIS DIMENSION PROVIDES FOR CLEARANCE BETWEEN THE FLANGE AND COMPONENTS ON THE MOTHERBOARD.

4. THIS DRAWING SHOWS THE DIMENSIONS OF THE STIFFENING FLANGE ONLY. SEE FIGURE 9-5 FOR DIMENSIONS OF THE REMAINING FEATURES.

5. TOLERANCE UNLESS OTHERWISE NOTED: ± 0.25 [± 0.010]

A-0919

Figure 11-10: Full Height I/O Bracket for Low Profile Cards

The form factor dimensions for a PCI Express DUAL-SLOT Add-in Card are shown in Figure 11-11. The only difference from standard height cards is the restricted component height on the primary side of the card.

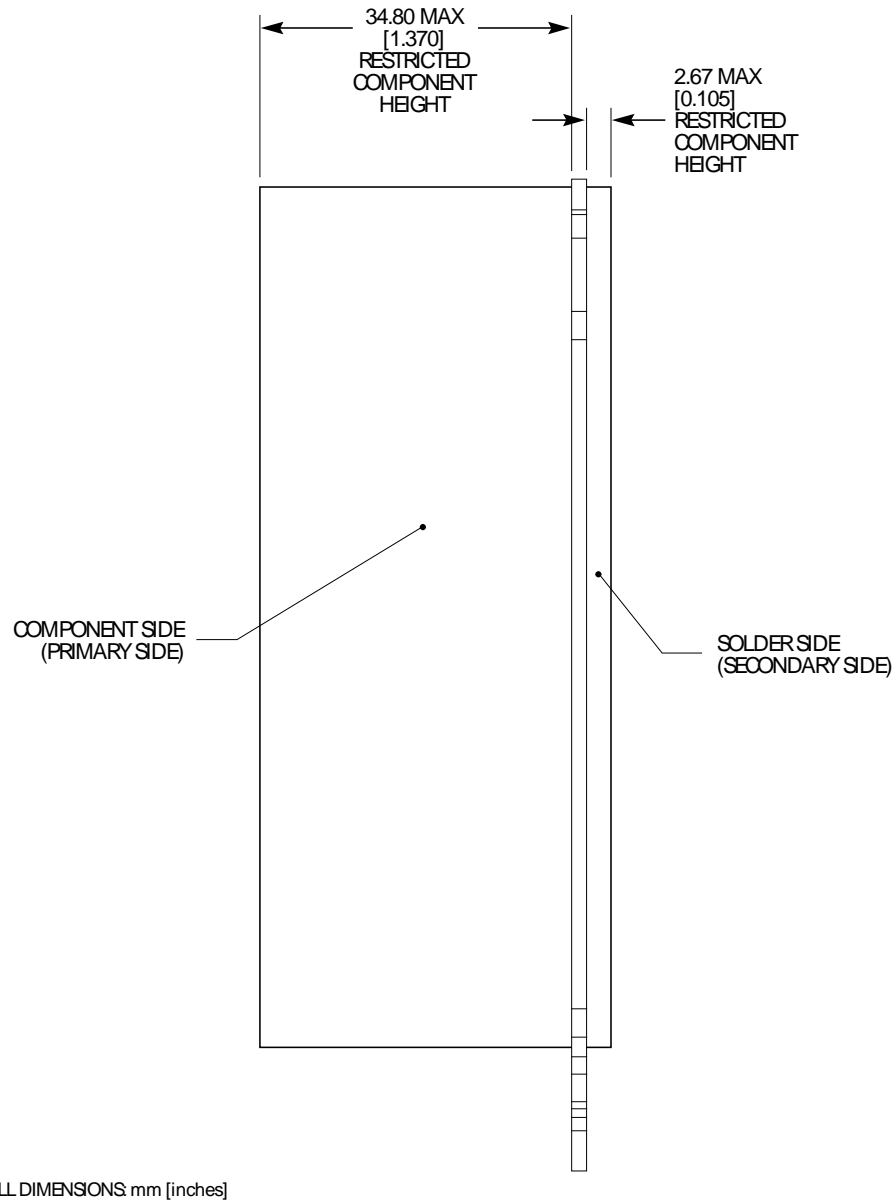


Figure 11-11: PCI Express DUAL-SLOT Add-in Card Dimensional Drawing

The form factor dimensions for a PCI Express TRIPLE-SLOT Add-in Card are shown in Figure 11-12. The only difference from standard height full-length cards is the additional spacing of the restricted component height on the primary side of the card.

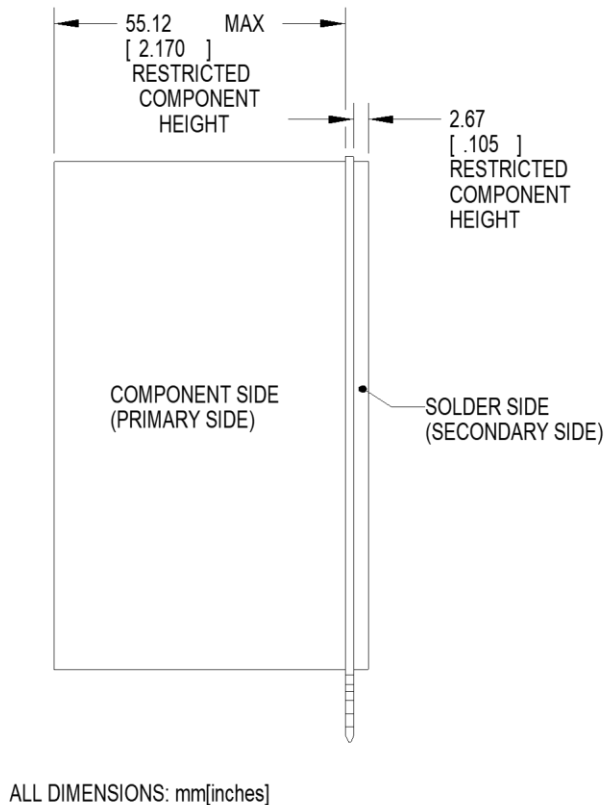
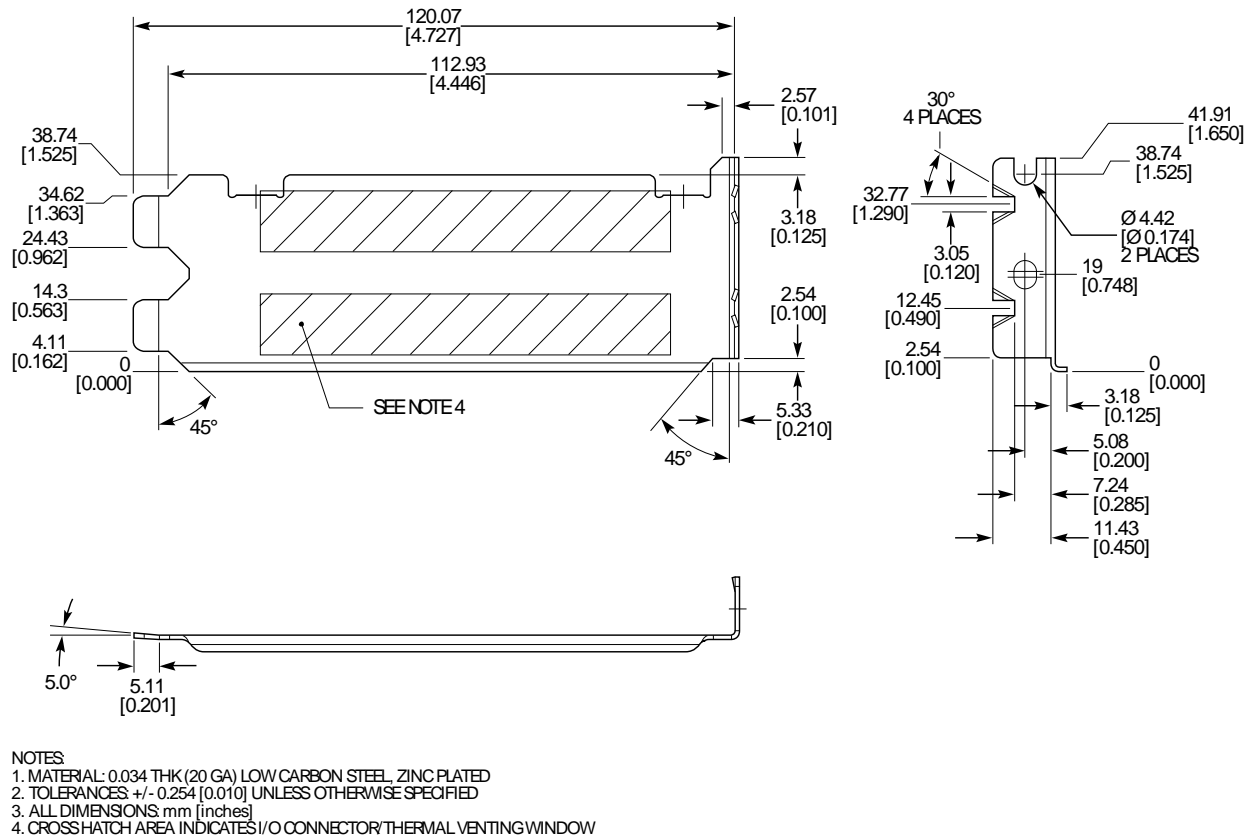


Figure 11-12: PCI Express TRIPLE-SLOT Add-in Card Dimensional Drawing

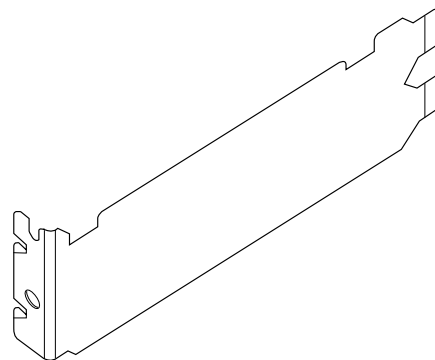
A PCI Express DUAL-SLOT Add-in Card may utilize a two slot I/O bracket to accommodate adequate thermal management.

Figure 11-13 is a detailed drawing of a two-slot I/O bracket design. Figure 11-14 is an isometric view of the two-slot I/O bracket with an area for Add-in Card venting. The size and number of any holes in the bracket follow proper EMI and thermal design guidelines.



A-0402

Figure 11-13: Detailed Two-Slot I/O Bracket Design

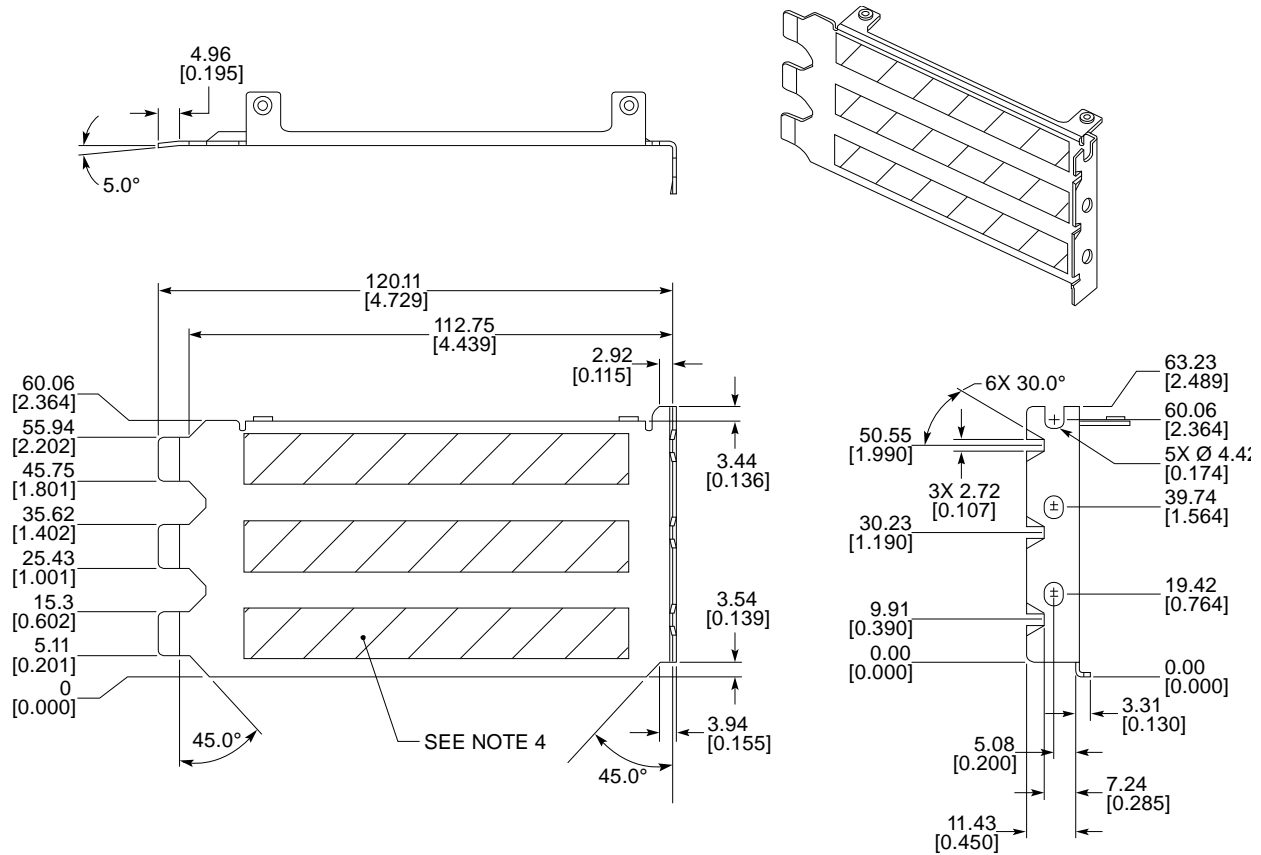


A-0403

Figure 11-14: Two-Slot I/O Bracket Example (Isometric View)

A PCI Express TRIPLE-SLOT Add-in Card may utilize a three slot I/O bracket to accommodate adequate thermal management.

Figure 11-15 is a detailed drawing of a three-slot I/O bracket design. Figure 11-16 is an isometric view of the three-slot I/O bracket with an area for Add-in Card venting. The size and number of any holes in the bracket follow proper EMI and thermal design guidelines.



NOTES:

1. MATERIAL: 0.034 THICK (20 GA) LOW CARBON STEEL, ZINC PLATED.
2. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.254 [0.010]
3. ALL DIMENSIONS: MM [INCHES].
4. CROSS HATCH AREA INDICATES I/O CONNECTOR/THERMAL VENTING WINDOW.

Figure 11-15: Detailed Three-Slot I/O Bracket Design

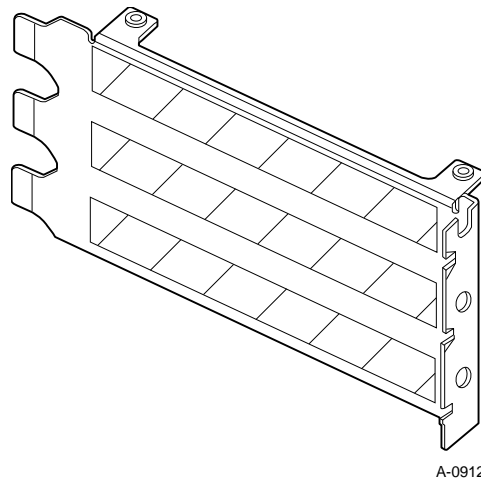


Figure 11-16: Three-Slot I/O Bracket Example (Isometric View)

PCI Express Add-in Cards require additional card retention and support for Add-in Cards that are greater than 350 grams in mass. Testing has shown that using the connector retention mechanism alone for Add-in Cards over 350 grams will cause connector and/or card damage.

Additionally, use of the “hockey stick” retention feature defined in this specification with certain Add-in Card thermal solutions makes access to and disengagement of the connector retention mechanism difficult without special tools. As a result, the “hockey stick” feature is optional for a PCI Express Add-in Card.



IMPLEMENTATION NOTE

PCI Express Usage of the “Hockey Stick” Feature

The hockey stick feature is optional for a PCI Express Add-in Card design. The actual board design used to omit this feature is implementation dependent, but the resultant layout cannot exceed any CEM outline measurement.

This specification defines keepouts and features on any PCI Express Add-in Card to be used for card retention. Detailed retention mechanism design, however, is considered implementation specific and it is up to system OEMs to work with card vendors.

The following guidelines must be observed when designing retention mechanism for high mass Add-in Cards:

- The use of the “hockey stick” feature alone is unlikely to be sufficient because of the high card mass allowed in this specification (1.5 kg maximum). The use of the keepout area to hold the card in place is strongly recommended. This mechanism may be necessary to prevent excessive deformation of the card during shock and vibration.
- The bracket is part of the card retention mechanism. It must have sufficient mechanical strength to withstand system-level shock and vibration. Deformation of card brackets has been one of the major failure mechanisms in the past.
- All cards shall be enabled for a full-length Add-in Card retainer. Partial length cards shall have means of being extended to full length and equipped with the retainer. The card features used for extending partial length cards to full length are the card vendor’s option; they may include component keepouts and holes similar to those shown in Figure 11-3.

- All cards shall be enabled for a full-length stiffener to minimize card flexure during dynamic events. When included, the stiffener must be located within the card component keep-in volume as defined in Figure 11-11 and Figure 11-12. Implementation details are the card vendor's option.
- A PCI Express card shall not exceed 1.5 kilograms in mass. To support such a mass, attention must be paid to bracket, chassis strengths, and retention mechanism designs. Card manufacturers must make efforts to minimize the card mass.

11.2. Add-in Card Layout Requirements and Recommendations

Operation at a data rate of 32.0 GT/s places requirements on the Add-in Card layout, specifically with respect to the edge-finger area of the board. These layout methods may also be used at data rates of 16.0 GT/s and below.

11.2.1. Core Shielding Ground Planes and Fingertip Ground Vias in Edge-Finger Areas

For an Add-in Card that supports 32.0 GT/s, there must be an inner layer ground under the edge-fingers in the high-speed region comprising pins A12/B12 and beyond. The inner layer ground plane must extend the full length of the edge-finger region from the main routing area of the Add-in Card. The inner layer grounding plane must lie at a depth of 0.52 mm (20.5 mil) or deeper beneath the edge-finger copper pads on the surface of the PCB (see Figure 11-17). This requirement applies to both sides of the Add-in Card, so a symmetric pair of shielding planes is used. These planes greatly reduce crosstalk between the Tx and Rx lanes in the edge-finger region. In the case of a high-layer count board multiple deep planes may lie within this region.

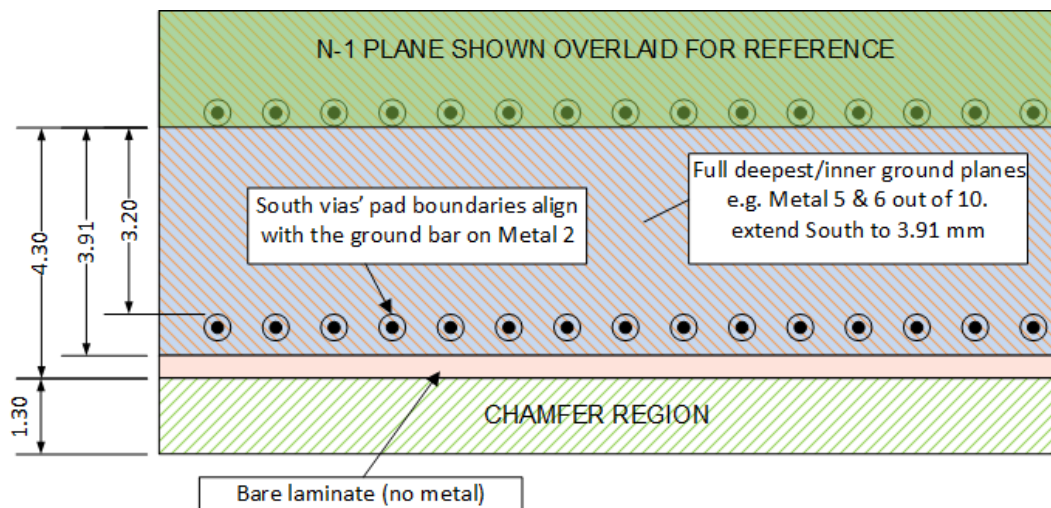


Figure 11-17: Detail of the Core Shielding Ground Plane beneath the Add-in Card Edge-Fingers

Additionally, for an Add-in Card that supports 32.0 GT/s, there must be a row of plated vias connected to the inner layer ground plane along the bottom of the edge-fingers in the high-speed region comprising pins A12/B12 and beyond. These vias are collectively known as Fingertip South Vias. Their position and size are shown in Figure 11-18. The vias must be plated through-holes (PTH) and may be shared among ground pads on both faces of the Add-in Card. The drill and pad size are not specified. Instead, the upper boundary of the via pad must align with the 3.20 mm dimension shown in Figure 11-18. Ground vias must be joined in the “I bar” with surface metal, as shown in the Figure 11-18. The vias should be center aligned with the gap between the pads, laterally offset from the edge-fingers by 0.50 mm.

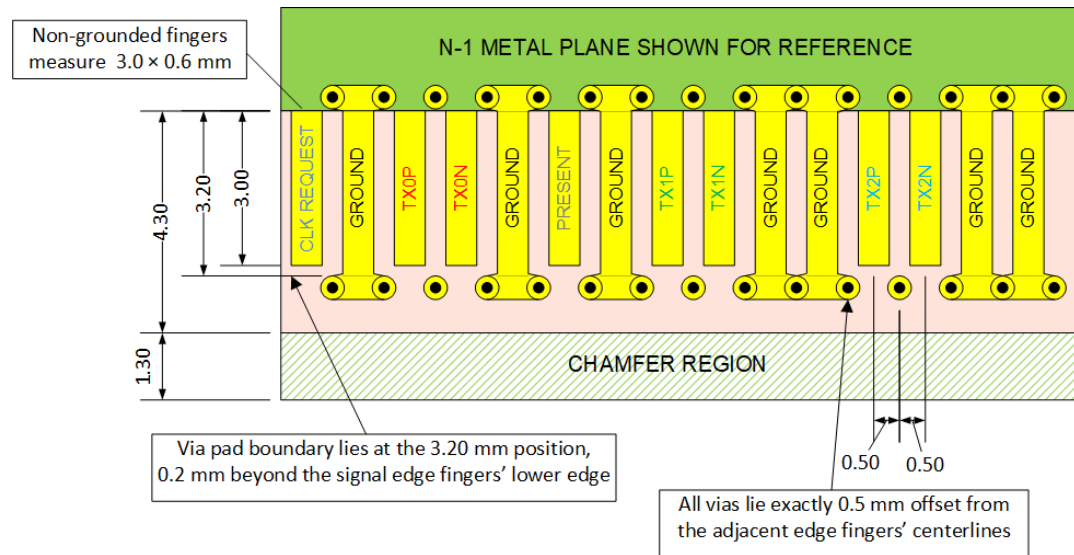


Figure 11-18: Add-in Card Edge-Finger Region, South Edge Ground Vias Indicated.
A portion of the N-1 plane (e.g. Metal 2) is shown for reference

A lateral ground bar must be implemented to join all the Fingertip South Vias on the first inner layer (N-1) on each side of the board (Metal 2, for example). The ground bar must align with the north edge of the vias at the 3.20 mm dimension indicated in Figure 11-19. The ground bar should be 0.71 mm (28 mil) wide. This ensures adequate clearance from the chamfer region.

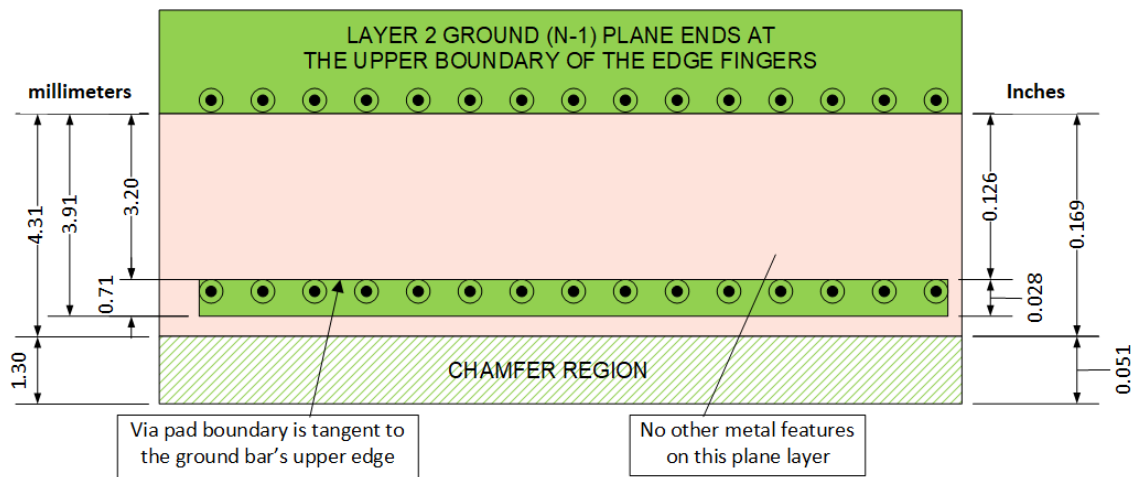


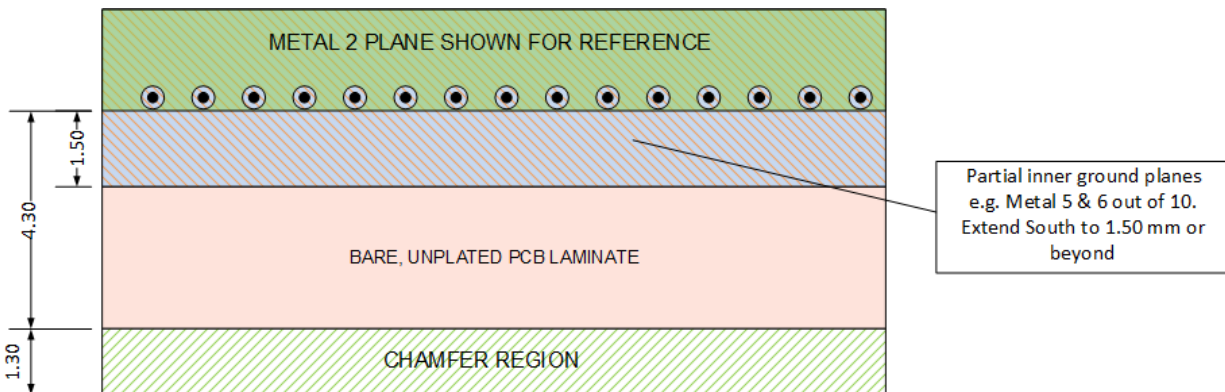
Figure 11-19: Detail of the N-1 Layer Geometry, Highlighting the Lateral South Ground Bar

11.2.1.1 Relaxed Requirements of Ground Planes and Ground Vias in Edge-Finger Area for Slower Data Rates

For an Add-in Card that supports only 16.0 GT/s and slower data rates, the requirements for the inner layer ground plane and south side vias may be relaxed as stated here.

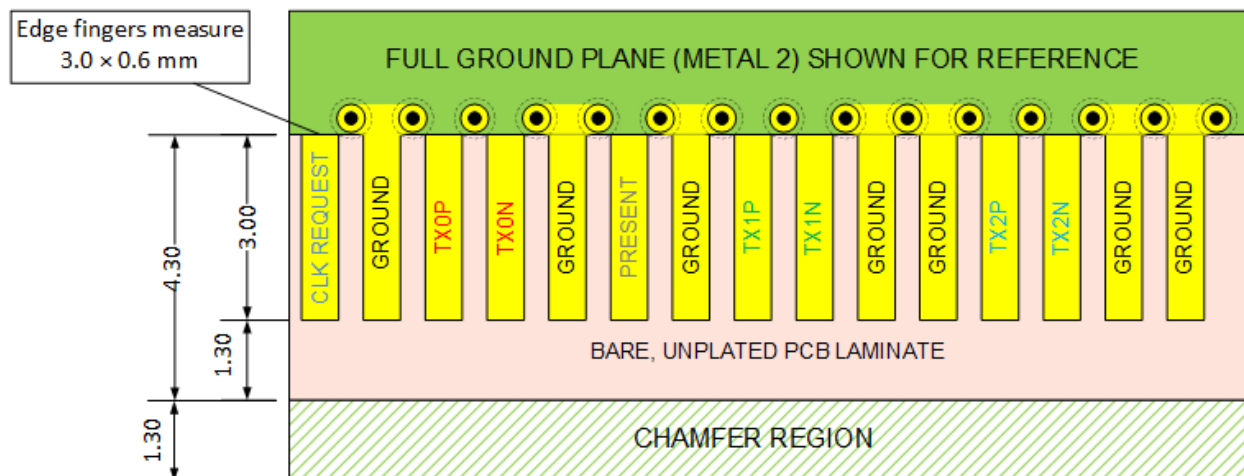
There must be an inner layer ground plane under the edge-fingers in the high-speed region comprising pins A12/B12 and beyond. The inner layer ground plane must extend at least $\frac{1}{2}$ the length of the edge-finger region from the main routing area of the board ($1.50 \text{ mm} \pm 0.038 \text{ mm}$) or longer. The inner layer ground plane must be at a depth of at least $0.520 \text{ mm} \pm 0.038 \text{ mm}$ or deeper beneath the edge-finger copper pads on the surface of the PCB (see Figure 11-20).

Additionally, for an Add-in Card that supports only 16.0 GT/s and slower data rates, there is no requirement for a row of Fingertip Ground Vias connecting to the inner layer ground plane along the bottom of the edge-fingers in the high-speed region comprising pins A12/B12 and beyond. Accordingly, there no requirement for the lateral ground bar on Layer N-1 at these lower data rates (see Figure 11-21).



Note: This pattern is permitted for 16 GT/s and below

Figure 11-20: Detail of the N-1 Layer Geometry, Highlighting the Lateral South Ground Bar



Note: This pattern is permitted for 16 GT/s and below

Figure 11-21: At Data Rates of 16.0 GT/s and below, all Edge-Fingers have the same Geometry, with no need for Fingertip South Vias or a layer N-1 Lateral South Ground Bar

11.2.2. Edge-Finger Length, Width, and Outer Layer Keepout

Edge-fingers that are not assigned to Ground in the region A12/B12 and beyond, are 3.00 mm in length and 0.60 mm width (± 0.038 mm) with the top of the edge-finger located 5.60 mm above the south edge of the Add-in Card edge. This creates a nominal 1.30 mm gap between the edge-finger and chamfer region.

Small amounts of residual surface metal are permitted in the region extending 0.13 mm beyond the lower end of the edge-finger. All PRSNT1# and PRSNT2# pins are now the same dimensions as all other edge-fingers. See Figure 11-22.

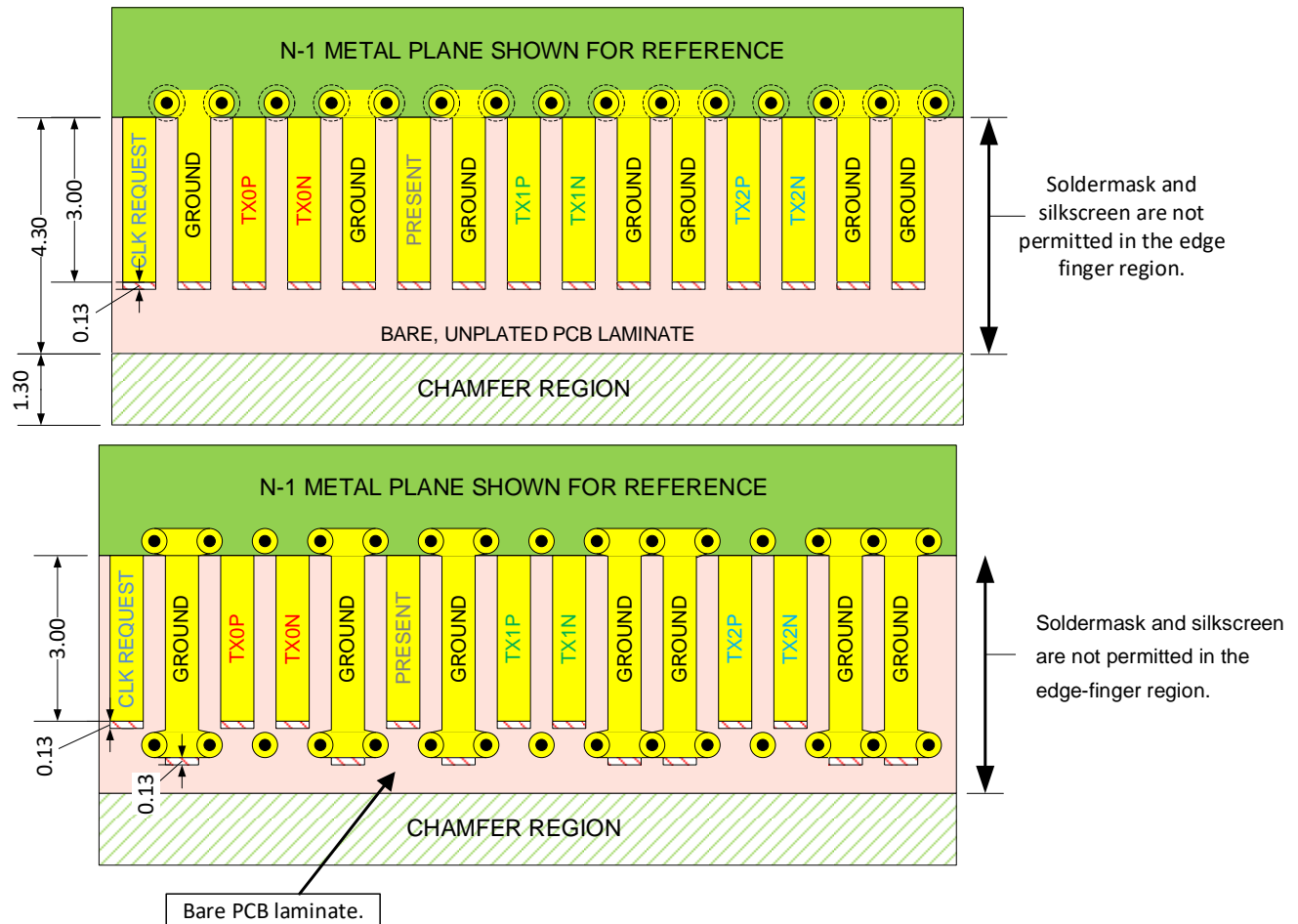


Figure 11-22: Add-in Card Edge-Fingers Indicating Edge-Finger Length and Surface Metal Keepout Areas

11.2.3. Add-in Card Adjacent North Edge-Finger Ground Vias

Add-in Card ground vias serving the north edge-finger ground conductors must be aligned with the gap between adjacent edge-fingers, to reduce obstruction to signals routed from non-ground edge-fingers. The axes of the North Ground vias must be no more than 0.38 mm (15 mil) from the boundary of the edge-finger pinfield. The edge-fingers must be connected to the ground via with a length of trace whose width matches or exceeds the via pad diameter to minimize the inductance of the ground connection (see Figure 11-23). North ground vias may be implemented as plated through-holes (PTH), and may be shared by edge-fingers assigned as ground pins on the front and back of the Add-in Card.

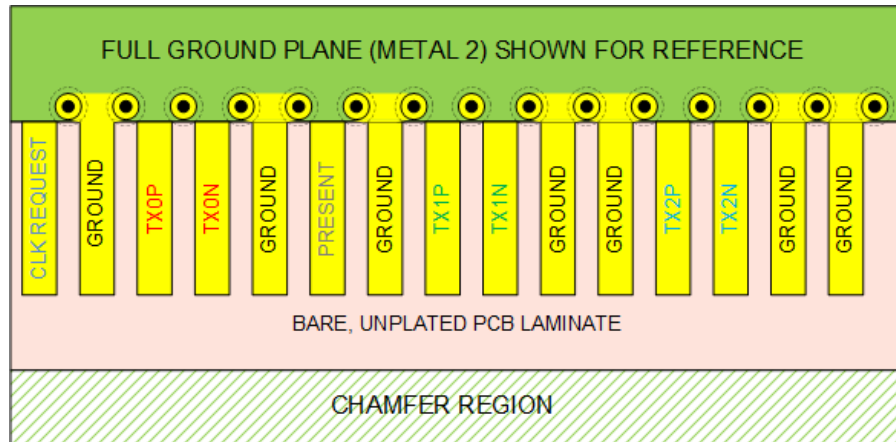


Figure 11-23: Add-in Card Edge-Fingers Indicating Adjacent North Edge-Finger, Ground Vias, North Ground Vias, and Joined Ground

This requirement improves signal integrity by increasing the frequency of a pathological ground resonance present in the ground conductors.

Many of the north ground edge-fingers are double grounds (two ground edge-fingers adjacent to each other on the same Add-in Card surface). In these cases, joining the adjacent edge-fingers at the via location is required to provide additional crosstalk reduction.

11.2.4. No Add-in Card Depopulated or Floating Edge-Fingers

Edge-fingers must be present in every pin position in the high-speed region comprising pins A12/B12 and beyond, even if the signals are not used on the Add-in Card or System Board. Having an edge finger present permits the implementation of the AC sideband termination on the Add-in Card. The only exception to this would be cards whose electrical length is smaller than the mechanical board outline. Therefore, every required edge-finger must be present and connected to either a high-speed Tx/Rx pair, a ground, or a sideband termination network. This requirement applies to edge-fingers assigned to ground, even if two ground fingers are adjacent. In all cases the uppermost appropriate PRSNT2# edge finger must be connected, in accordance with Chapter 3.

Implementation Note: An example of a card whose electrical length is smaller than the mechanical board outline would be: A card having a x4 electrical width, while having a x16 mechanical length that fully engages a x16 slot, may install edge-fingers only in those positions required for a x4 card. In this case the edge-fingers in positions A12 to A32, and B12 to B32, must all be present and connected, with no depopulated fingers among them. The edge-finger positions A33 to A82 and B33 to B82 may be depopulated.

11.2.5. Auxiliary Signal Conductor AC Match Termination

Several auxiliary (sideband) signals lie among high-speed Tx/Rx pairs and ground conductors in the range of pins A11/B11 to A82/B82.

Within this section of the connector pinfield, and the corresponding Add-in Card edge-finger region, some of the auxiliary signals, such as CLKREQ#, PWRBRK#, are used; while others, such as RSVD, are unused. In all cases, these conductors are naturally terminated in a mismatched impedance at each end, which may present a short, an open, or a high impedance, unless explicit matching is applied.

Poorly terminated pins allow resonances that degrade insertion loss and markedly increases high frequency crosstalk for adjacent high-speed Tx/Rx signal pairs.

These resonances result from the conductive structure comprising the system board via (or SMT pad), the connector contact, and the Add-in Card edge-finger. The resonances effectively couple energy to and from the high-speed lanes and the sideband lanes, which may interfere with the assigned function of these signals.

The Add-in Card can reduce these resonances, and the resulting high frequency crosstalk, by terminating the conductors through a controlled impedance to ground. However, to avoid compromising any low frequency signaling on these auxiliary conductors a DC blocking capacitor must be added to the termination.

Thus, all conductors carrying these auxiliary signals must be terminated by a circuit consisting of an appropriate resistor (nominally $42.5\ \Omega \pm 10\%$) in series with an appropriate capacitor (nominally $1.0\ \text{pF} \pm 20\%$) to ground.



Note: All Add-in Cards are required to terminate sideband conductors to an appropriate resistor and capacitor.

The following list of the auxiliary signals must be terminated:

- A x1 Add-in Card or connector requires two auxiliary signals be terminated:
 - B12 CLKREQ#
 - B17 PRSNT2#
- A x4 Add-in Card or connector requires all x1 card signals plus four additional auxiliary signals be terminated:
 - A19 MFG
 - A32 RSVD
 - B30 PWRBRK#
 - B31 PRSNT2#
- A x8 Add-in Card or connector requires all x4 card signals plus two more auxiliary signals be terminated:
 - A33 RSVD
 - B48 PRSNT2#
- A x16 Add-in Card or connector requires all x8 card signals plus three additional auxiliary signals be terminated:
 - A50 RSVD
 - B81 PRSNT2#
 - B82 RSVD

The trace length from the top of an auxiliary signal edge-finger to the DC blocking capacitor in the termination circuit must be as short as practicable, but no maximum length is specified. This trace shall be impedance matched in the range of 42.5 Ω from the edge-finger to the DC blocking capacitor. The ground via for the termination network must lie within 1.0 mm (39.4 mil) of the resistor component pad/through-hole.

Schematic connectivity for the B-side pins is shown for a x16 Add-in Card in Figure 11-24. Corresponding A-side connectivity is required but is not shown.

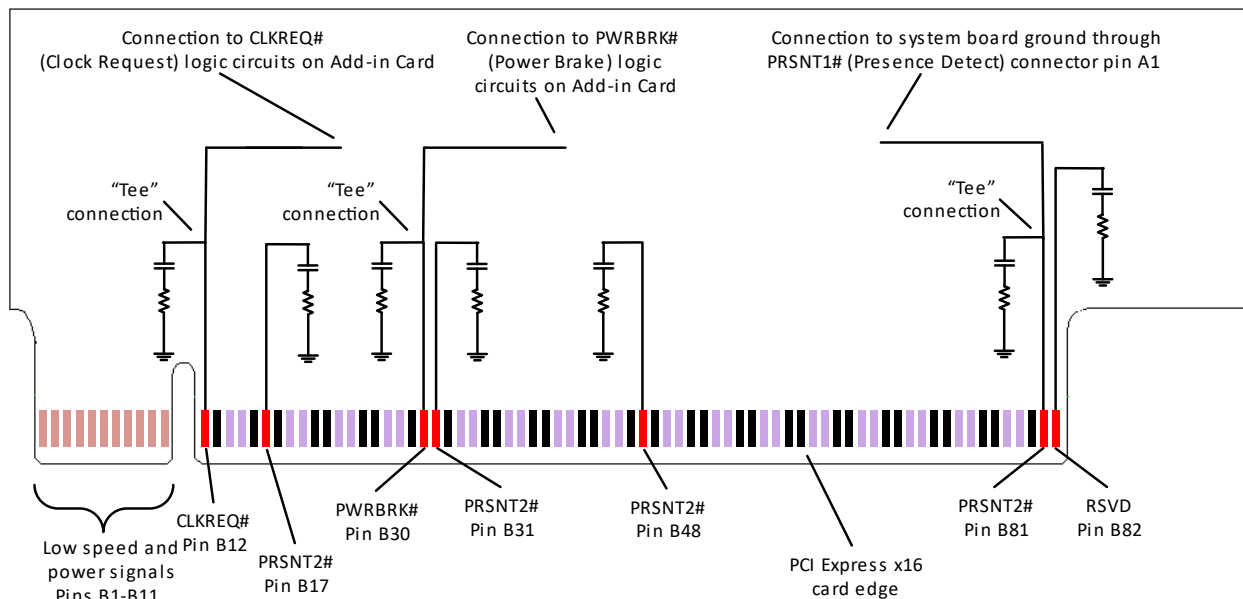


Figure 11-24. x16 Add-in Card with AC Terminations on All Auxiliary and Reserved Signal Conductors (B-side only)

The AC sideband termination provides a matched termination to ground for floating conductors such as RSVD and some PRSNT2# pins. Other auxiliary pins effectively have a tee connection. The path between the PRSNT1# and PRSNT2# pad B81, is one example of a sideband signal that will have a tee connection to the AC termination.

Add-in Cards supporting 8.0 GT/s or lower data rates also benefit from AC sideband termination, but to a lesser degree. AC sideband termination should not adversely affect functionality on legacy mating PCIe system boards.



Note: The DC blocking capacitors used here for the auxiliary signal terminations are not the same as those used on the high-speed differential TX pairs specified by C_{TX} in the *PCI Express® Base Specification*.

11.3. System Board Layout Requirements and Recommendations

Operating at a data rate of 16.0 GT/s or higher places additional requirements on the system board layout. System boards that do not support 16.0 GT/s or higher, may optionally implement any or all these requirements. For system boards, all the requirements in this section, pertaining to each data rate that is supported, must be met.

11.3.1. Sentry Ground Vias Adjacent to Auxiliary Signal Vias

This requirement is mandatory for the system boards mounting through-hole/press-fit connectors operating at 16.0 GT/s. It does not apply to system boards mounting surface mount connectors.

Due to the irregular signal assignment within the CEM connector pinfield, markedly higher crosstalk and degraded insertion loss are observed among high-speed Tx and Rx signal pairs adjacent to auxiliary signal pins. This crosstalk stems chiefly from the distribution of signal, ground, and sideband vias in the system boards' pinfield.

To mitigate this effect, small diameter through-hole ground vias called "sentry vias" must be placed adjacent to each auxiliary signal pin via on the system board, in the range A12/B12 to A82/B82. For ease of routing other signals laterally through the pinfield, the via drill diameter should be small (e.g., 0.25-0.30 mm (10-12 mil)).

Two, three, or four sentry vias must be used for each auxiliary signal via. The sentry vias must be placed adjacent to the auxiliary signal via, within the limits of the PCB fabrication for technology used to construct the system board.

Figure 11-25a illustrates a x4 CEM connector pinfield with three or four sentry vias flanking each auxiliary signal. Note that this implementation exceeds the minimum sentry via requirement; as few as two sentry vias per pin may be used, as shown in Figure 11-25b.

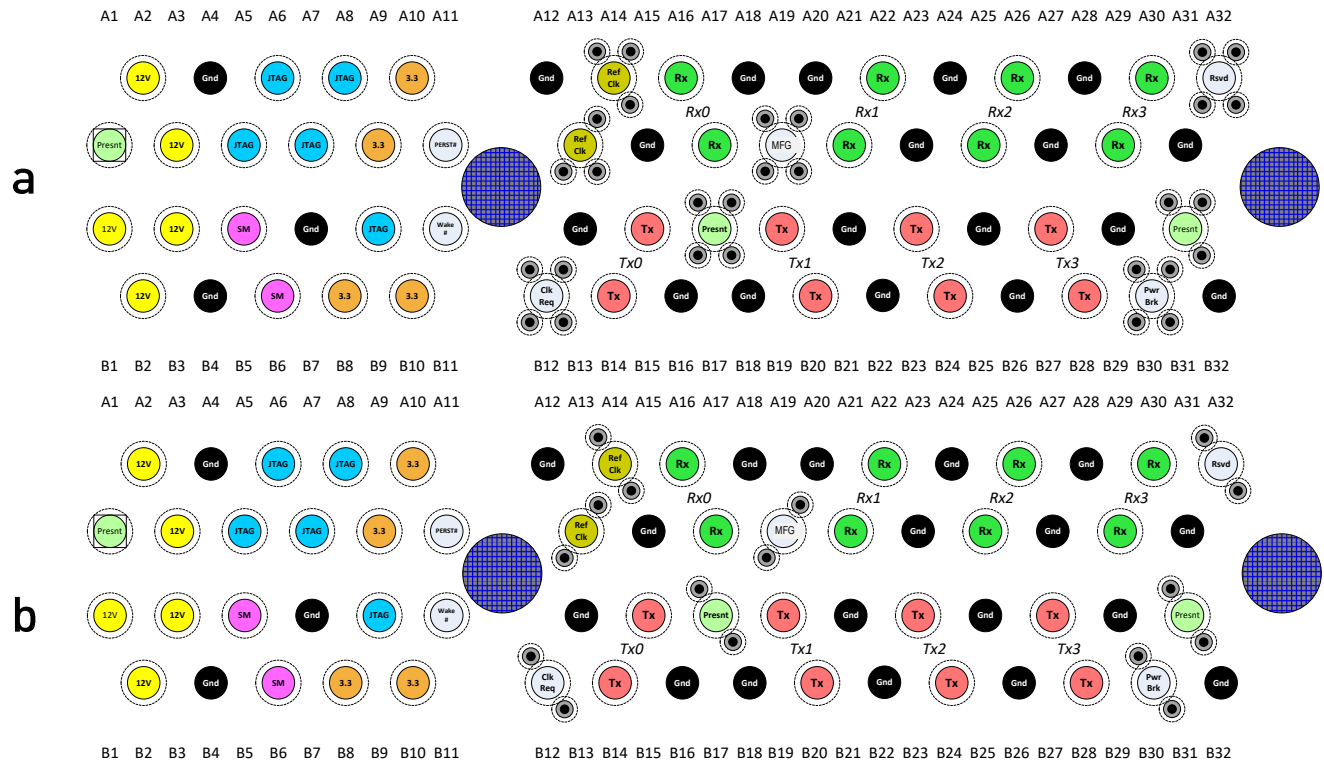


Figure 11-25: System Board with Sentry Vias for All Auxiliary Signal Vias for a x4 system board: a) Four sentry vias per pin. b) Two sentry vias per pin

A x1 connector requires four auxiliary signals be isolated with Sentry vias:

- CLKREQ# (pin B12)
- REFCLK+ (pin A13)
- REFCLK- (pin A14)
- PRSNT2# (pin B17)

A x4 connector requires four more auxiliary signals be isolated:

- MFG (pin A19)
- RSVD (pin A32)
- PWRBRK# (pin B30)
- PRSNT2# (pin B31).

A x8 connector requires two more auxiliary signals be isolated:

- RSVD (pin A33)
- PRSNT2# (pin B48)

A x16 connector requires three more auxiliary signals be isolated

- RSVD (pin A50)
- PRSNT2# (pin B81)
- RSVD (pin B82)

Sentry vias must be present on these pins, regardless of whether the auxiliary pin is in use. In general, any auxiliary pins that are in use operate at such low data rates that any bandwidth-limiting effects of adjacent ground vias will not affect the assigned function of the pin. Sentry vias must not be applied to the highspeed Tx and Rx pinfield vias since this will markedly degrade performance. Sentry vias need not be applied to grounds. Surface mount connectors do not require sentry vias.

System boards supporting only 8.0 GT/s or below, will benefit from sentry vias, but to a lesser extent. When present, sentry vias will not adversely affect operation at any data rate.

11.3.2. System Board Requirements for 32.0 GT/s Operation

Every system board that supports 32.0 GT/s operation must use surface mount (SMT) PCI Express connectors.

CEM 5.0 introduces the surface mount connector footprint that has multiple updates and new requirements. The pin field lies on a 1.0 mm pitch, with pad dimensions of 0.53 x 2.00 mm (see Figure 11-26).

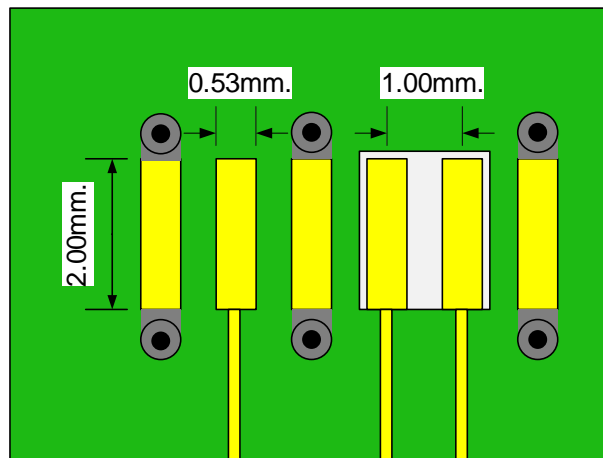


Figure 11-26. System Board PCI Express Connector SMT Footprint, Highlighting Pad Size and Pin Pitch

In the high-speed region (pins A12/B12 and beyond), all ground SMT pads must have adjacent ground vias, one at the “Toe” and one at the “Heel”. The ground vias must be placed as close as possible to the ground pads, within the limits of the process technologies used to manufacture and assemble the boards. Via-in-pad is not required. Reference via dimensions and locations are shown in Figure 11-27.

Broad 0.53 mm wide connecting trace and oversize 0.53 mm surface pads are shown, matching the width of the SMT pads. No drill diameter requirements are specified.

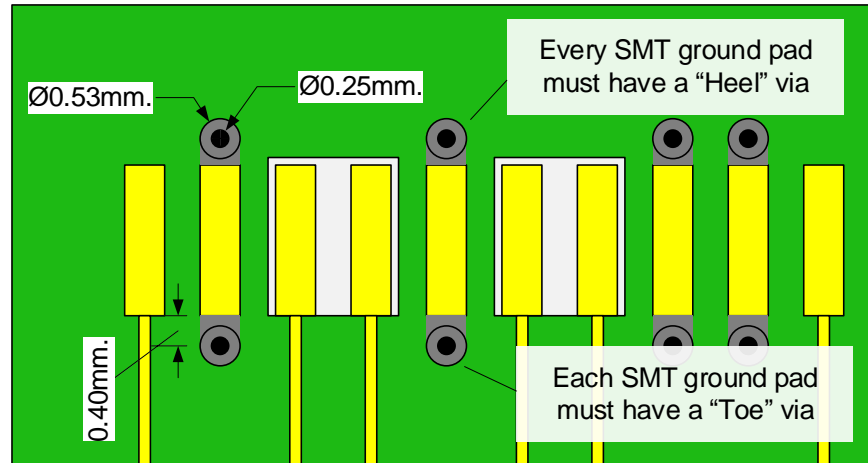


Figure 11-27. System Board PCI Express Connector SMT Footprint, Highlighting the Location of Heel and Toe Ground Vias

In the high-speed region (pins A12/B12 and beyond), all high-speed pairs must have ground plane voiding in the adjacent plane layer. Representative void dimensions are shown in Figure 11-28. These dimensions may be adjusted to accommodate different system board stackups.

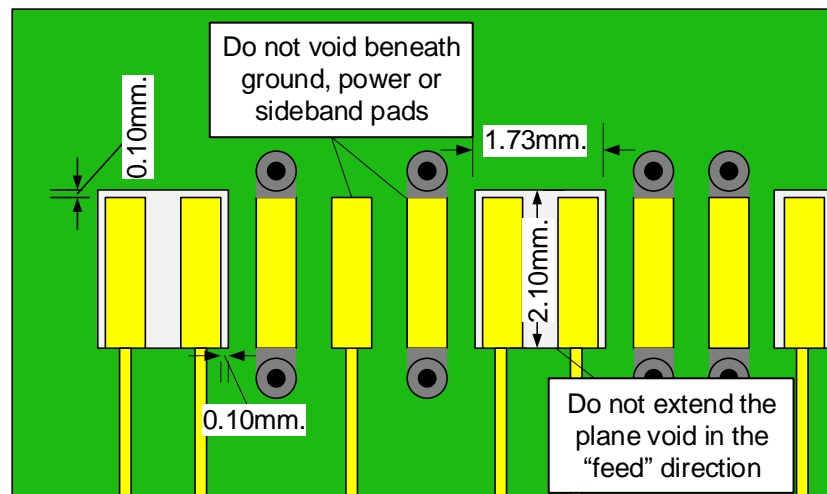


Figure 11-28. System Board PCI Express Connector SMT Footprint, Highlighting the Suggested Voiding Scheme for High-speed Pairs

11.3.3. Auxillary Signal Conductor Termination

To reduce crosstalk onto high-speed signals, all conductors carrying auxillary signals are recommended to be terminated as described in Section 11.2.5.

11.4. Connector and Add-in Card Locations

Figure 11-29 shows an example of a typical desktop system (microATX form factor). The Add-in Card slots are PCI and AGP Add-in Card connectors.

The PCI Express Add-in Cards use the space allocated for those Add-in Card slots to take advantage of the existing chassis infrastructure. This requirement dictates that the PCI Express connectors must use the slots that coincide with the locations of the present PCI and AGP slots/connectors. The following examples show cases where some of the PCI and AGP connectors are replaced by PCI Express connectors. While not shown, it is permitted that all connectors may be replaced by PCI Express connectors.

Figure 11-30 illustrates the introduction of a PCI Express connector in a microATX system, co-existing with the PCI connectors. In this case, the PCI Express connector is introduced by replacing the AGP connector.

Like the PCI Add-in Card, the components on a PCI Express Add-in Card face away from the CPU, or the core area.

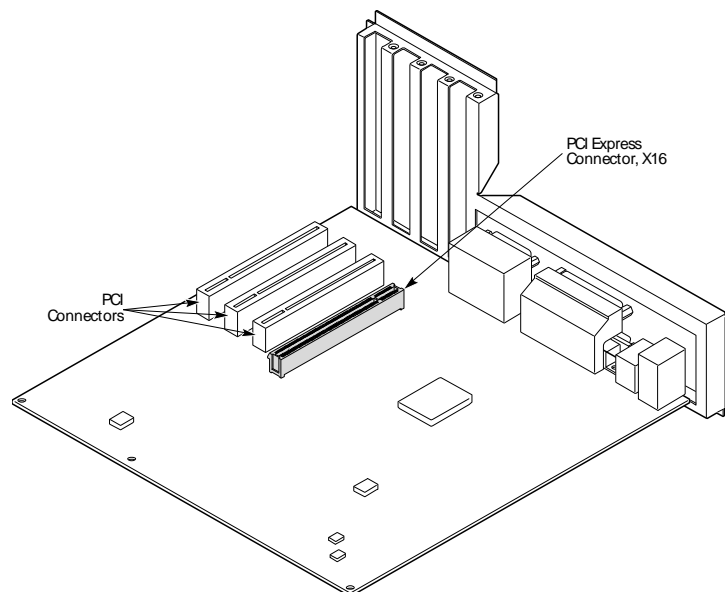


Figure 11-29: Example of a System in microATX Form Factor

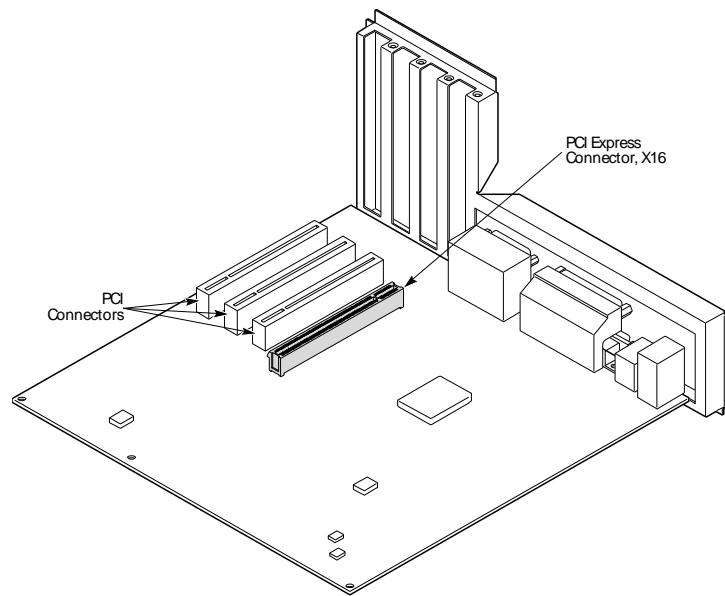
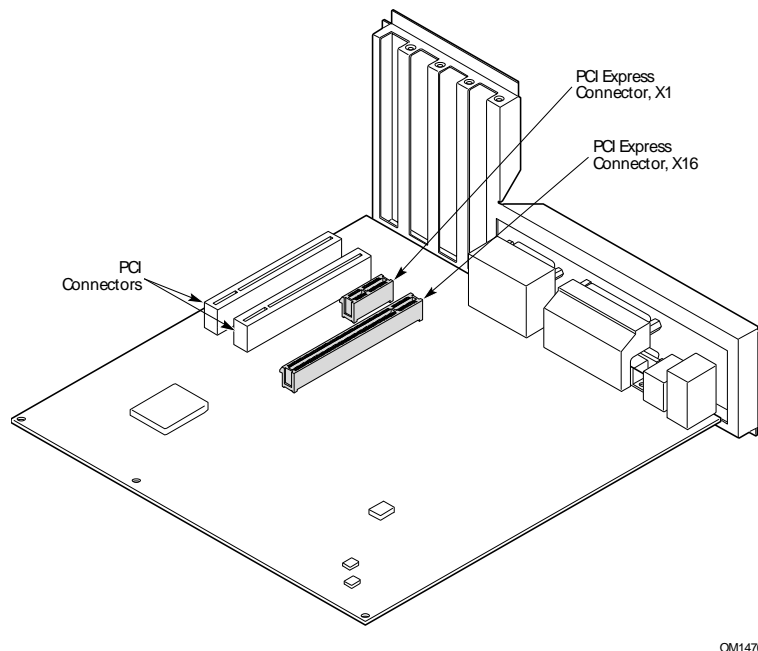


Figure 11-30: Introduction of a PCI Express Connector in a microATX System

Over time, PCI Express connectors have replaced PCI connectors in most applications, and AGP has largely fallen into disuse on the system board. Figure 11-31 shows a situation where a basic bandwidth (x1) PCI Express connector replaces a PCI connector (x1) and a high bandwidth (x16) PCI Express connector replaces the AGP connector.



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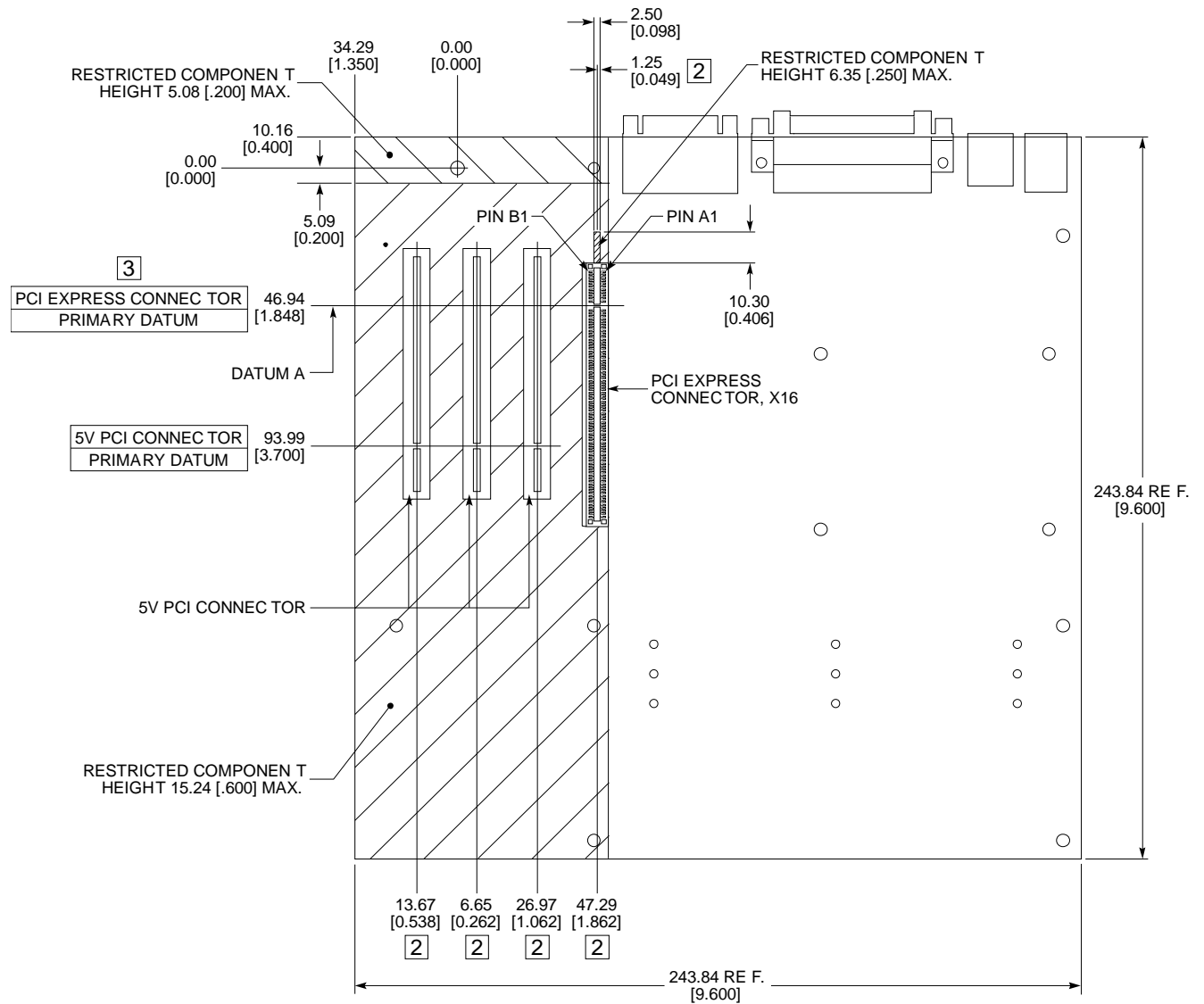
Figure 11-31: Introduction of More PCI Express Connectors on a microATX System

Figure 11-32 shows the PCI Express connector location, as well as the component height restriction zones. In this case, a x16 PCI Express connector replaces the AGP connector. When more PCI Express connectors are introduced, the height restriction zones will grow accordingly. This is depicted in Figure 11-33, where an additional x1 PCI Express connector is introduced along with the x16 connector. The 5.08 mm (0.200 inches) maximum and the 15.24 mm (0.600 inches) maximum height restriction zones are identical to the PCI requirements. However, the additional, small height restriction zones of 6.35 mm (0.250 inches) maximum are unique to PCI Express.

There is a slight offset between PCI and PCI Express connector locations. The PCI Express connectors are located slightly further away from the rear of the chassis. PCI Express Add-in Cards (see Note 2 in Figure 11-1A and Figure 11-6A) have a blocking tab to prevent them from being mistakenly inserted into a PCI slot. This feature requires the additional height restriction zones of 6.35 mm (0.250 inches) maximum.

The card retention clip requires additional height restrictions. Such restrictions depend on the retention clip design and location, which may vary from user to user. Since retention clip designs vary, they are not specified here as a requirement. However, in the design guideline, a reference retention clip design and implementation is given, together with the keepout and height restriction zones.

See Figure 11-34 and Figure 11-35 for standard height and low-profile connector openings in the chassis.



NOTES:

1. TOLERANCE UNLESS OTHERWISE SPECIFIED: $\pm .25$ [$\pm .010$]

NOTES:

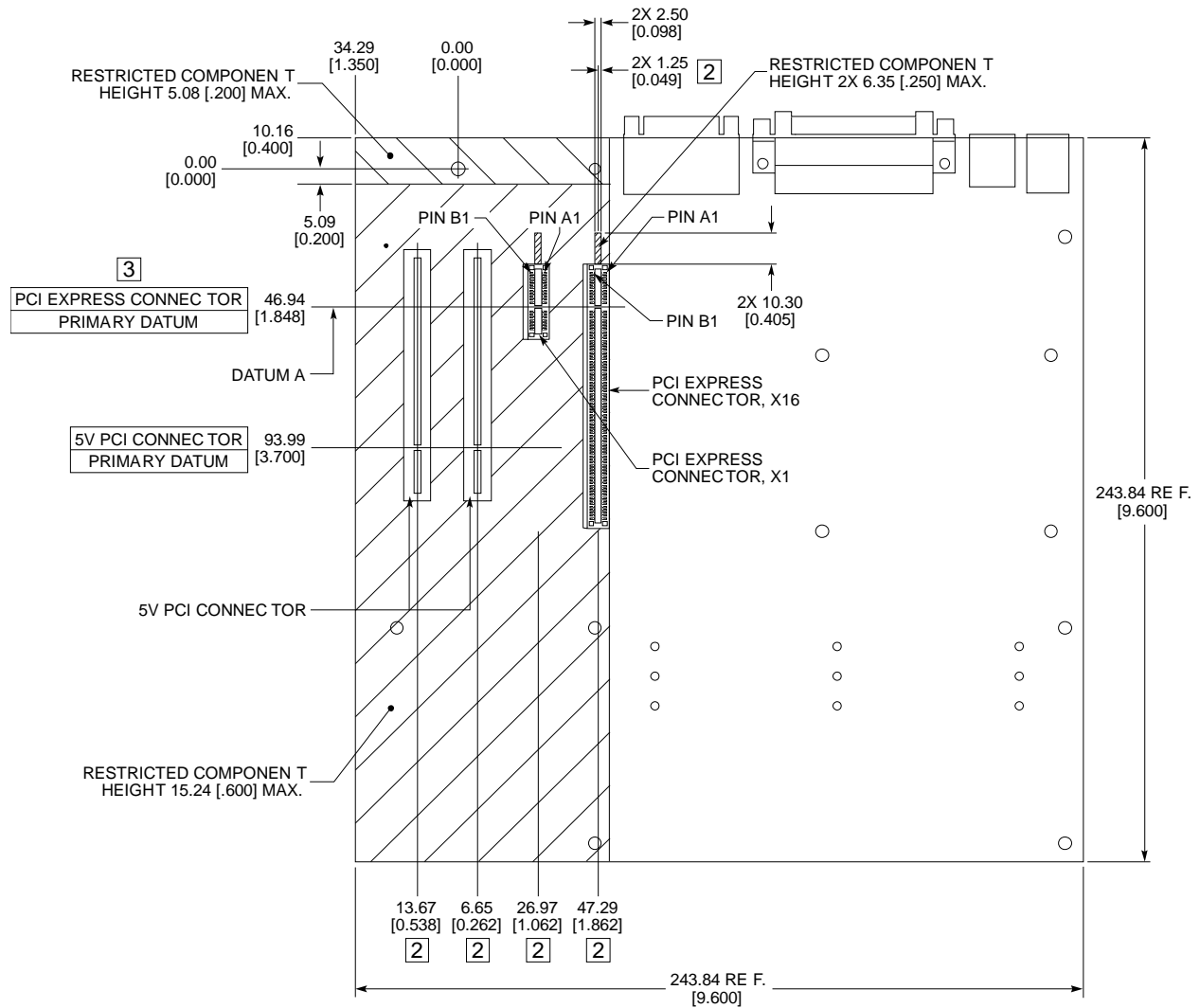
1. TOLERANCE UNLESS OTHERWISE SPECIFIED IS $\pm .25$ [$\pm .010$]

2. CENTER LINE OF CONNECTOR

3. THE PRIMARY DATUM IS THE DATUM **- A -** ON THE CONNECTOR (SEE FIGURE 33)

A-0913

Figure 11-32: PCI Express Connector Location in a microATX System with One PCI Express Connector

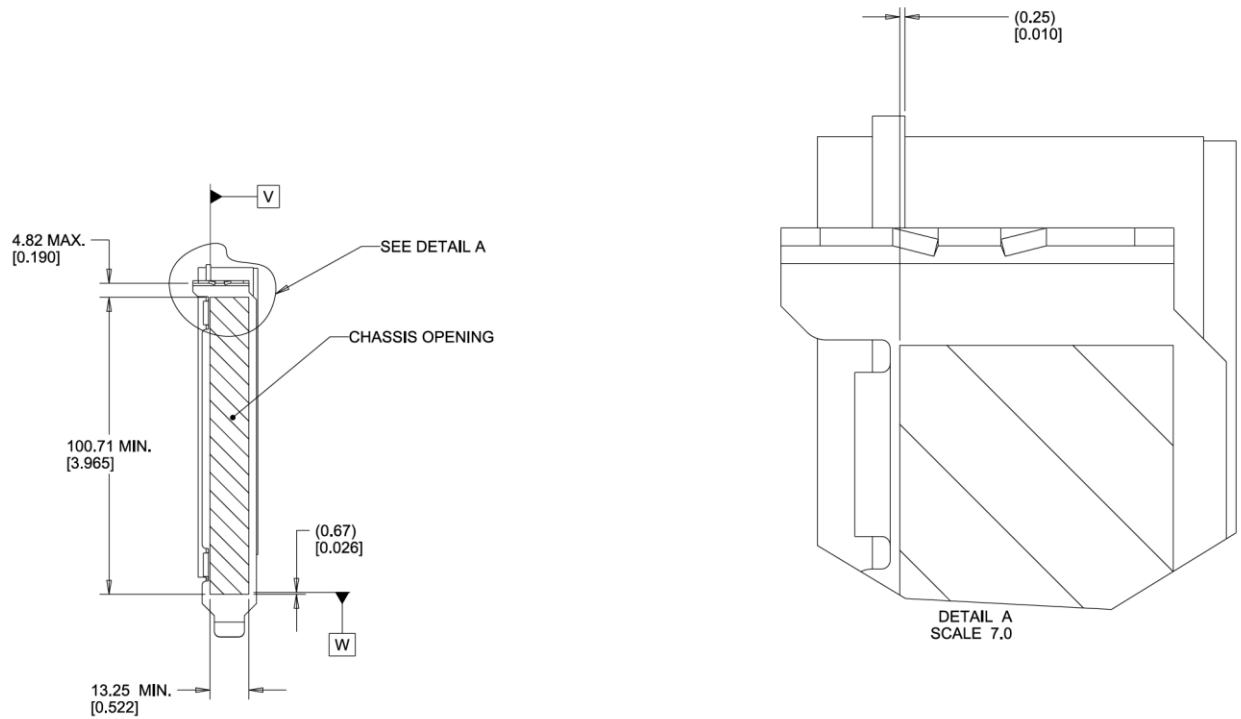


NOTES:

1. TOLERANCE UNLESS OTHERWISE SPECIFIED IS $\pm .25$ [$\pm .010$]
2. CENTER LINE OF CONNECTOR
3. THE PRIMARY DATUM IS THE DATUM **A** ON THE CONNECTOR (SEE FIGURE 33)

A-0914

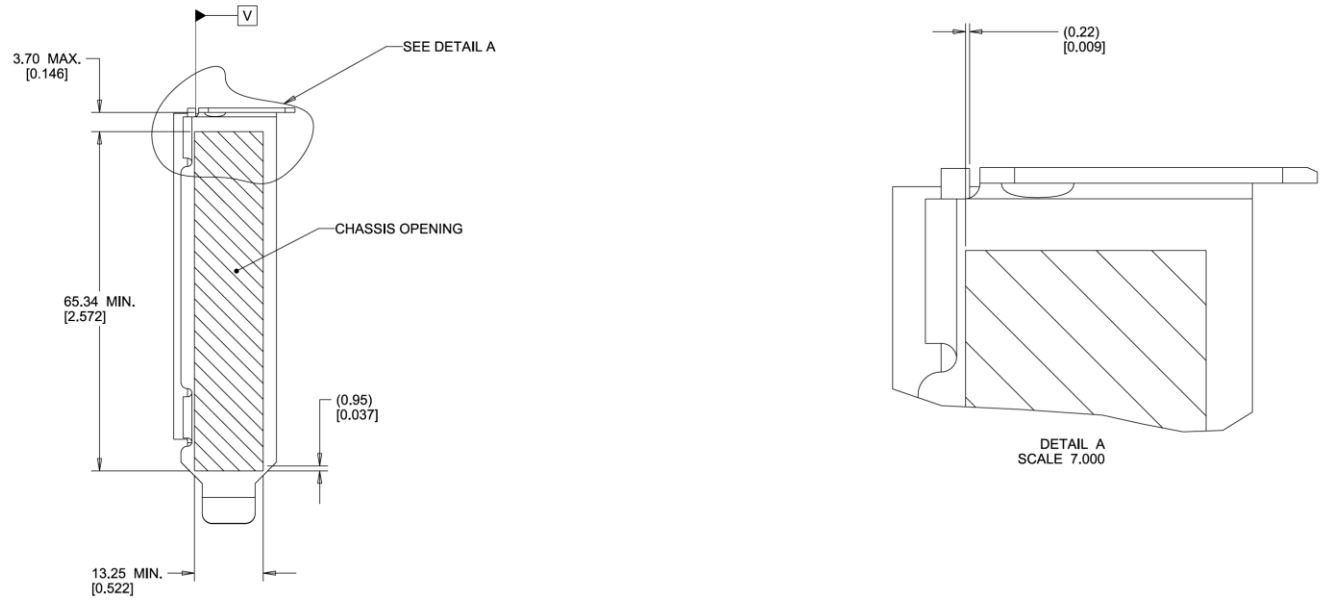
Figure 11-33: PCI Express Connector Location in a microATX System with Two PCI Express Connectors



NOTES:

1. CHASSIS OPENING IS THE MINIMUM REQUIRED APERTURE, TAKING INTO ACCOUNT REFERENCE SYSTEM LEVEL TOLERANCES. ACTUAL DIMENSIONS WILL VARY BASED ON SYSTEM IMPLEMENTATION.
2. THE SIZE OF THIS CHASSIS OPENING MUST INCLUDE SYSTEM ACCOMODATIONS, INCLUDING BUT NOT BE LIMITED TO: PROTRUDING CONNECTORS ON THE ADD-IN CARD, INSERTION AND REMOVAL OF THE ADD-IN CARD FROM THE SYSTEM, ETC.
3. I/O CONNECTORS MATING TO THE CARD CAN HAVE OVERMOLDS EXTENDING IN ALL DIRECTIONS AROUND THIS OPENING. THIS WILL LIMIT THE EFFECTIVE THICKNESS OF THE CHASSIS NEAR THIS REGION.

Figure 11-34: Standard Height Connector Opening in Chassis



NOTES:

1. CHASSIS OPENING IS THE MINIMUM REQUIRED APERTURE, TAKING INTO ACCOUNT REFERENCE SYSTEM LEVEL TOLERANCES. ACTUAL DIMENSIONS WILL VARY BASED ON SYSTEM IMPLEMENTATION.
2. THE SIZE OF THIS CHASSIS OPENING MUST INCLUDE SYSTEM ACCOMODATIONS, INCLUDING BUT NOT BE LIMITED TO: PROTRUDING CONNECTORS ON THE ADD-IN CARD, INSERTION AND REMOVAL OF THE ADD-IN CARD FROM THE SYSTEM, ETC.
3. I/O CONNECTORS MATING TO THE CARD CAN HAVE OVERMOLDS EXTENDING IN ALL DIRECTIONS AROUND THIS OPENING. THIS WILL LIMIT THE EFFECTIVE THICKNESS OF THE CHASSIS NEAR THIS REGION.

Figure 11-35: Low Profile Connector Opening in Chassis

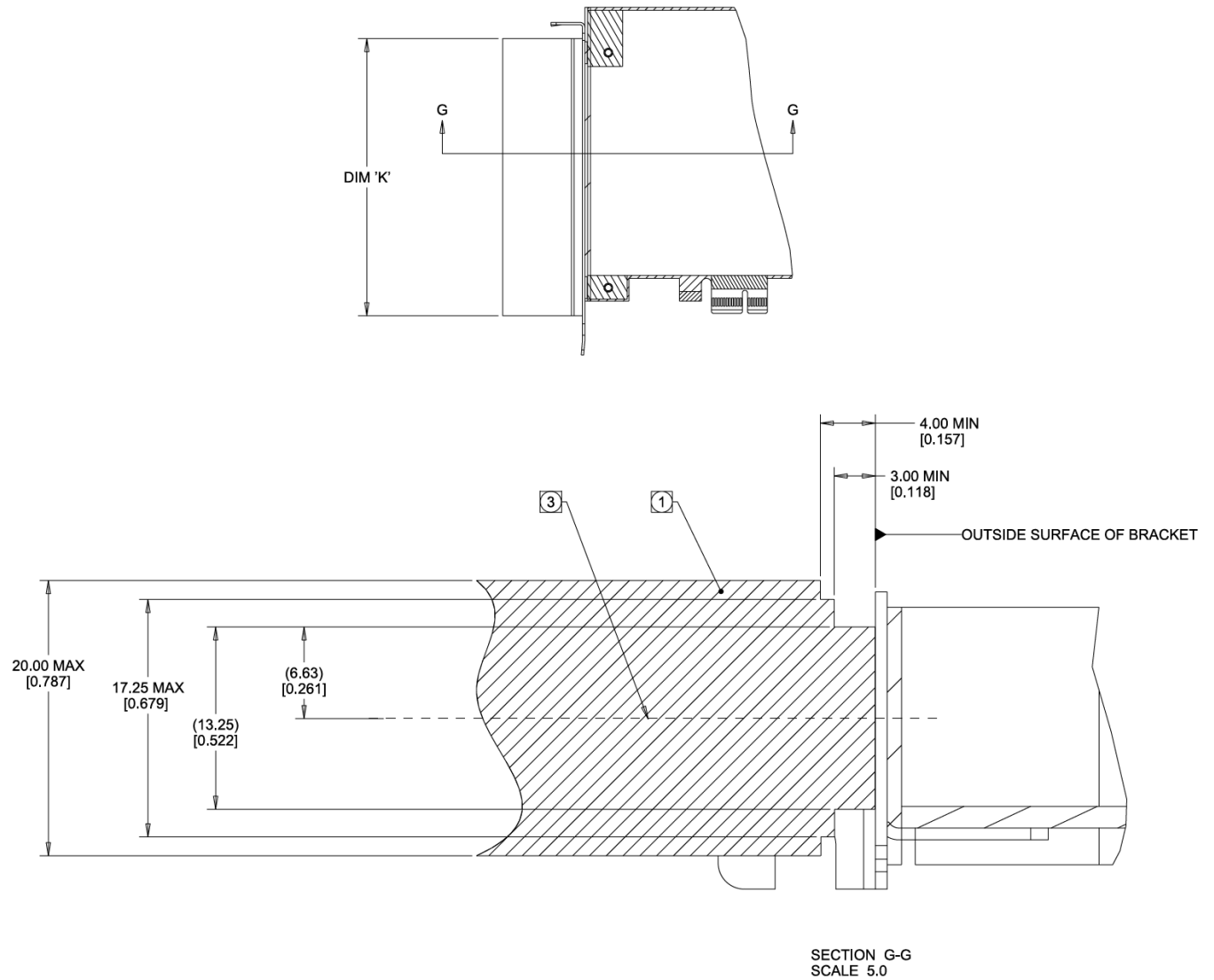


TABLE	
CARD HEIGHT	DIM 'K'
STANDARD HEIGHT (SEE FIGURE 6-17)	100.71 REF. [3.965]
LOW PROFILE (SEE FIGURE 6-18)	65.34 REF. [2.572]

NOTES:

① THE VOLUMETRIC CHASSIS KEEPOUT SHOWN REPRESENTS THE CLEARANCE REQUIRED TO ENABLE FULL MATING OF CABLE ASSEMBLIES TO I/O CONNECTORS ON THE ADD-IN CARD.

2. THE DESCRIBED VOLUME IS THE MINIMUM REQUIRED. ACTUAL DIMENSIONS WILL VARY BASED ON SYSTEM IMPLEMENTATION.

③ CENTERLINE EXTENDED PERPENDICULAR TO CHASSIS OPENING MID POINT

Figure 11-36: Chassis I/O Cable Keepout

Figure 11-37 and Figure 11-38 and shows examples of structure shapes that could affect cable attachment. Chassis wall thickness greater than the ATX wall thickness and the use of structural shapes formed in the chassis wall between slots (as shown) also affect cable attachment.

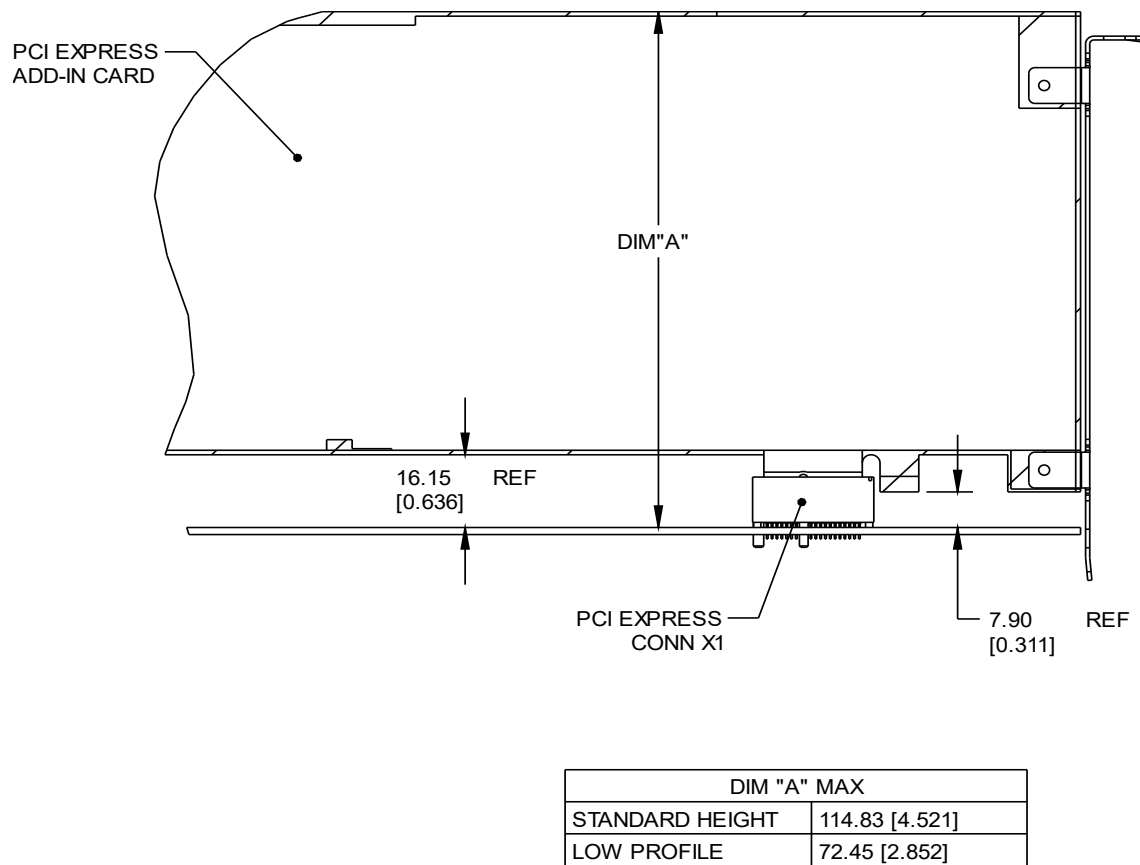
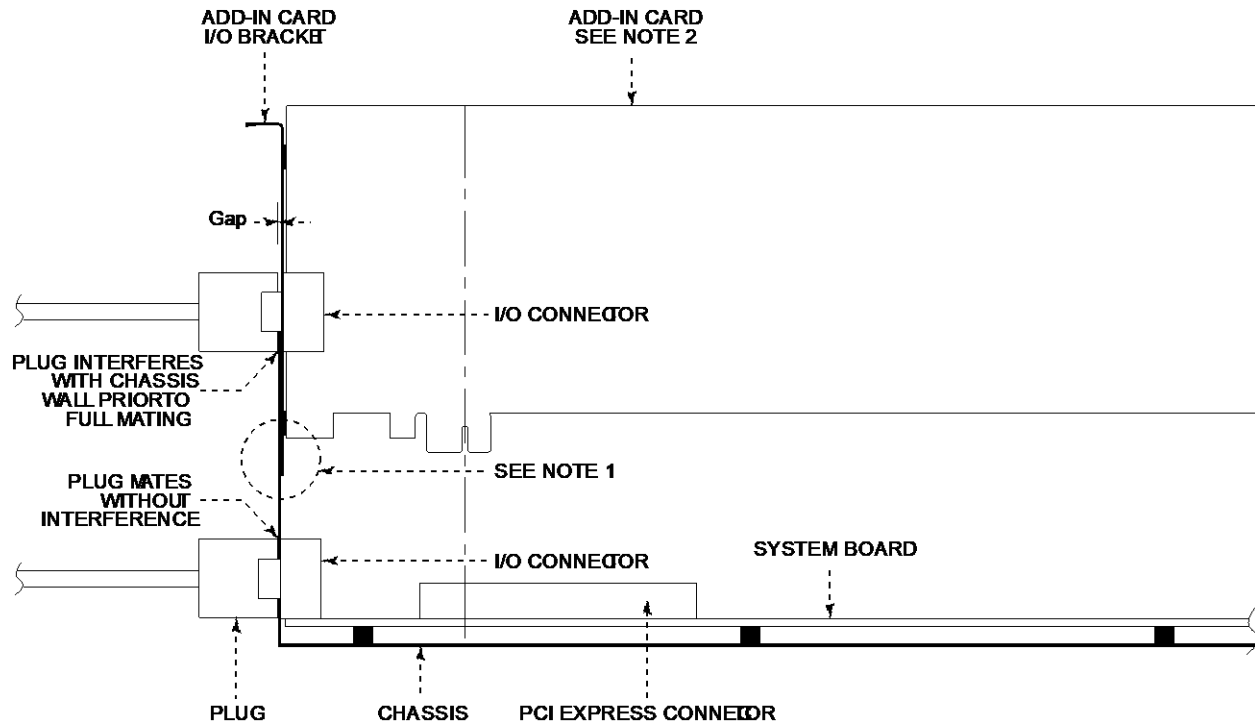


Figure 11-37: Impact of Structural Shapes



NOTES:

1. AS THE ADD-IN-CARD BRACKET RESIDES BEHIND THE CHASSIS WALL WHEN INSTALLED IN THE SYSTEM BOARD CONNECTOR, THE RESULTING DOUBLE WALL THICKNESS REDUCES THE PROTRUSION OF THE I/O CONNECTOR SUCH THAT THE CABLE PLUG MAY NOT FULLY MATE. SEE Figure 11-34 AND Figure 11-35 FOR MINIMUM CHASSIS CLEARANCE GUIDANCE. SEE Figure 11-36 FOR CHASSIS KEEPOUT/VCABLE + PLUG KEEP-IN VOLUMETRIC DEFINITION.
2. ADDITIONAL TOLERANCE FROM OTHER SOURCES (PCI EXPRESS CONNECTOR-TO-SYSTEM BOARD, ETC.).
3. ADD-IN-CARDS ARE UNIVERSAL. THEREFORE ADD-IN-CARD DESIGNERS MUST ASSUME THAT ADEQUATE CLEARANCE FOR I/O MATING CABLE PLUGS WILL BE PROVIDED IN THE SYSTEM. SEE Figure 11-34, Figure 11-35, AND Figure 11-36 FOR ADDITIONAL DETAILS ON THE NEEDED CLEARANCE.

A-0918

Figure 11-38: Impact of Structural Shapes in the System

11.5. Card Interoperability

PCI Express cards and connectors exist with a variety of Link widths. The interoperability of cards and connectors is summarized in Table 11-2.

Table 11-2: Card Interoperability

Card	Connector			
	x1	x4	x8	x16
x1	Required	Required	Required	Required
x4	No	Required	Required	Required
x8	No	No	Required	Required
x16	No	No	No	Required

The connectors columns refer to the PCI Express connectors mounted on a system board (see Chapter 6). The shaded area in Table 11-2 represents up-plugging, while the cells marked “No” represent down-plugging. Be aware of the following:

- Down-plugging, i.e., plugging a larger edge size card into a smaller connector, is not allowed and is physically prevented.
- Up-plugging, i.e., plugging a smaller edge size card into a larger connector, is supported.
- All PCI Express Add-in Cards must be able to negotiate and operate in all smaller Link widths from the full Link width down to x1. The x2 and x12 Link widths are optional.
- The upstream PCI Express components on a system board must be able to negotiate and operate in all smaller Link widths from the full Link width down to x1. The x2 and x12 Link widths are optional.

12. Add-in Card Thermal Reporting

Add-in Cards are influenced by the temperature and airflow velocity and volume present across these cards. To enable enclosure management to comprehend whether a given Add-in Card without integrated air movers can be adequately cooled based on its dynamic operating conditions, an Add-in Card is permitted to communicate its operating requirements over a range of environmental conditions through Vital Product Data (VPD). For Add-in Cards with a PCI Express Multi-Function Device that supports Thermal Reporting data using VPD, the data must be present in only Function 0. For multi-device Add-in Cards, the data must be present in only one of the PCI Express devices on the Add-in Card.

Platform software may read these values to determine whether an Add-in Card can be supported based on the Add-in Card's thermal characteristics as well as to determine how to optimize cooling mechanisms to ensure correct operation without expending excessive power on cooling.

Add-in Card Thermal Reporting uses three graph sets that each define up to 15 operating curves. Each curve corresponds to one numeric value communicated by the corresponding VPD field. Values associated with unspecified curves are treated as Reserved.

12.1. Airflow Impedance (AFI) Level

The intent of Airflow Impedance Level information is to identify Add-in Cards which, if in the same airflow path as other platform features to be cooled, may contribute to a total airflow impedance that impacts the cooling for the platform. Also, the installation of higher impedance Add-in Cards, especially if multiple such Add-in Cards are installed, in a platform may exceed the capabilities for a given platform fan's performance curve. Through testing, platform developers determine what Add-in Card AFI Levels the platform supports.

Impedance is categorized as one of N levels communicated by the Air Flow Impedance (AFI) Level field. Each level corresponds to one of the curves illustrated in Figure 12-1. The level is assigned based on the highest AFI level number which is still below the measured Add-in Card AFI throughout the range of air flows. The AFI Level field is defined for a value of 1 through 9 (inclusive). All other values are Reserved. See Table 12-1 for encoding.

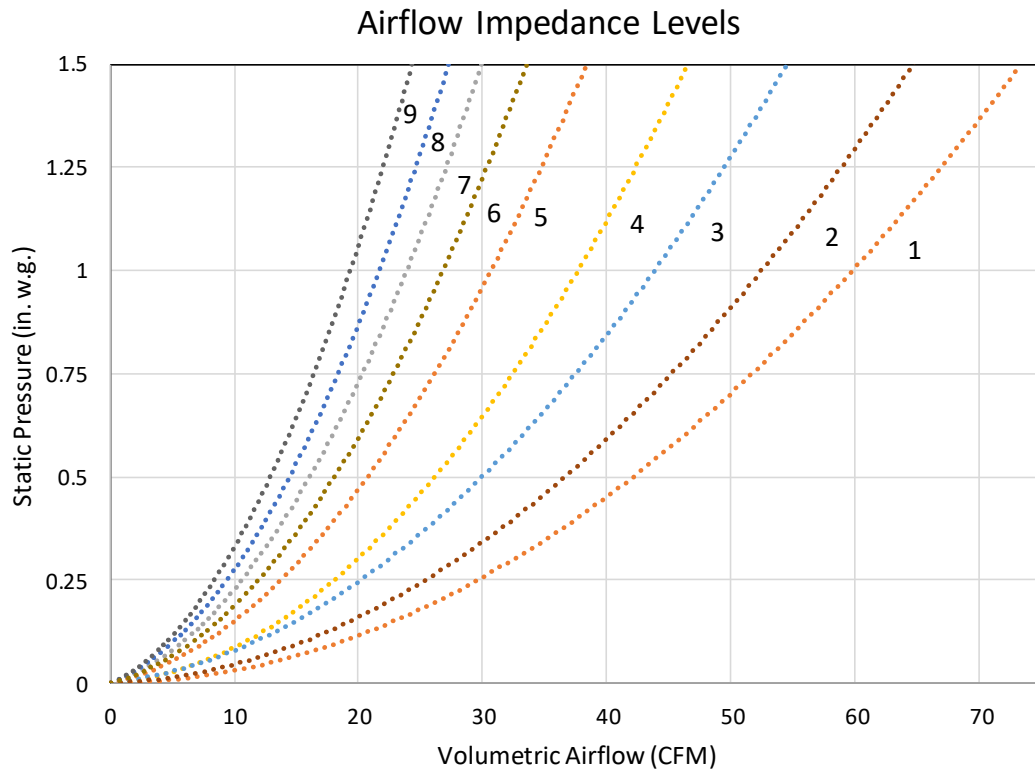


Figure 12-1. AFI Levels

An Add-in Card is to be rated to its appropriate AFI Level by comparing its measured impedance, in 0.25-inch water increments through the static pressure range of 0.25 to 1.25 in.w.g., to the AFI Level equations listed in Table 12-1. The lowest AFI Level which always has higher volumetric airflow for a given static pressure relative to the Add-in Card's measured impedance shall be listed as the Add-in Card's AFI Level.

The airflow impedance testing for an Add-in Card begins at 0.25 in.w.g. to lessen the potential for error at low flowrates.

Table 12-1. AFI Level Equations

AFI Level	Equation (X=volumetric airflow [CFM]; Y=static pressure [in.w.g.])
0	Reserved
1	$Y = 0.0003 * X^2 + 0.0003 * X$
2	$Y = 0.0003 * X^2 + 0.0012 * X$
3	$Y = 0.0004 * X^2 + 0.0035 * X$
4	$Y = 0.0006 * X^2 + 0.0023 * X$
5	$Y = 0.0008 * X^2 + 0.0066 * X$
6	$Y = 0.0011 * X^2 + 0.078 * X$
7	$Y = 0.0014 * X^2 + 0.0091 * X$
8	$Y = 0.0016 * X^2 + 0.0117 * X$
9	$Y = 0.0020 * X^2 + 0.078 * X$
10-15	Reserved

12.2. Maximum Thermal (MaxTherm) Level

The intent of the Maximum Thermal (MaxTherm) Level information is to define the minimum airflow required at a given air temperature for which an Add-in Card, when stressed to its Thermal Design Power (TDP) level limit, will operate within its component's reliability limits and without degraded Add-in Card performance.

Once an Add-in Card's thermal performance profile is established (see Appendix C), the Maximum Thermal (MaxTherm) Level is determined. MaxTherm is the lowest curve in Figure 12-2 which is entirely above the Add-in Card's quantified thermal performance curve throughout the range of approach ambient temperatures – also referred to as local ambient temperatures – shown on the X-axis ranging from 25 °C up to 65 °C.

Note that the curves shown in Figure 12-2 and Figure 12-3 are for reference only. Compare measured readings against the equations defined in Table 12-2. Note that Thermal Levels 2, 3, and 4 have a low limit for their approach air speed of 100 LFM, meaning their Thermal Levels do not require an Add-in Card to support less than 100 LFM.

It is recommended, that Add-in Card developers strive to offer solutions that can operate within the shaded recommended design space envelope shown in Figure 12-2 to maximize the number of systems that can support such conditions.

The MaxTherm field is defined for a value of 1 through 8 (inclusive). All other values are Reserved. See Table 12-2 for encodings. Platform software must treat a Reserved MaxTherm value as if MaxTherm reporting was not supported.

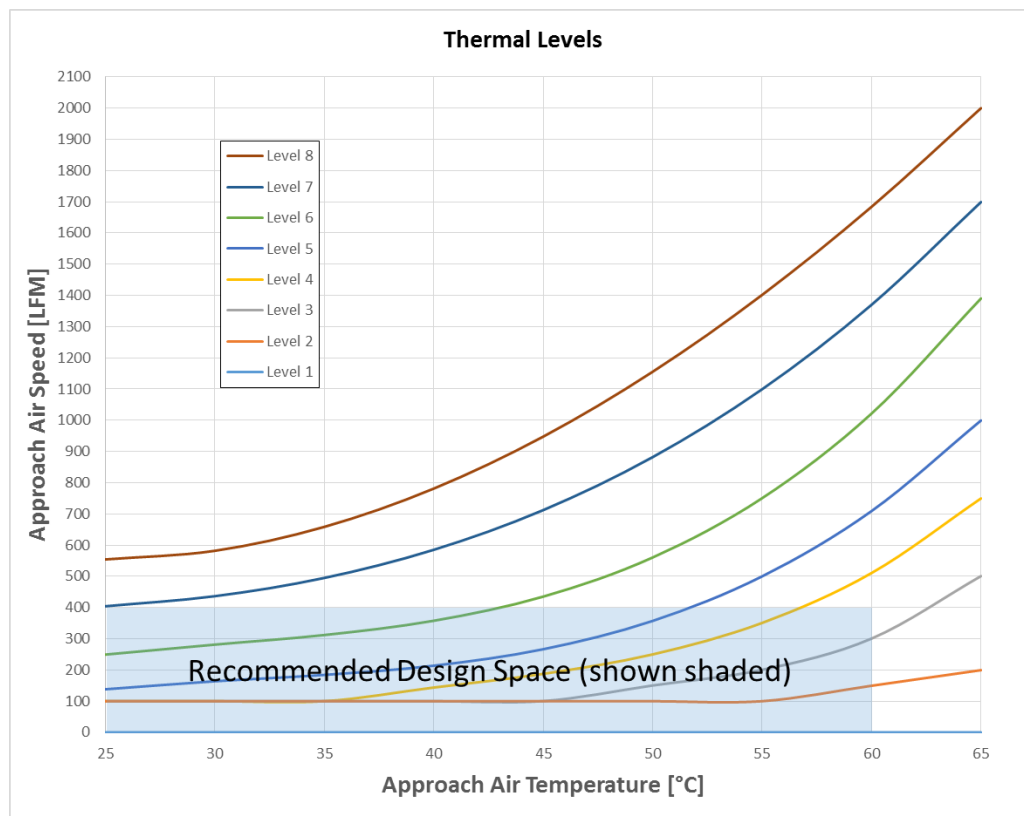


Figure 12-2. MaxTherm and DTherm Levels

No lower air speeds shall be presumed for approach air temperatures below 25 °C.

For example, Figure 12-3 illustrates the curve of a hypothetical Add-in Card that has been tested. Given this profile, the MaxTherm Level for the unit under test (UUT) Add-in Card would be set to 6 if it wished to support the entire temperature range up through 65 °C. The highlight circle in the figure shows it exceeds MaxTherm Level 5 above an approach air temperature of 52 °C. Table 12-2 lists the thermal level equations.

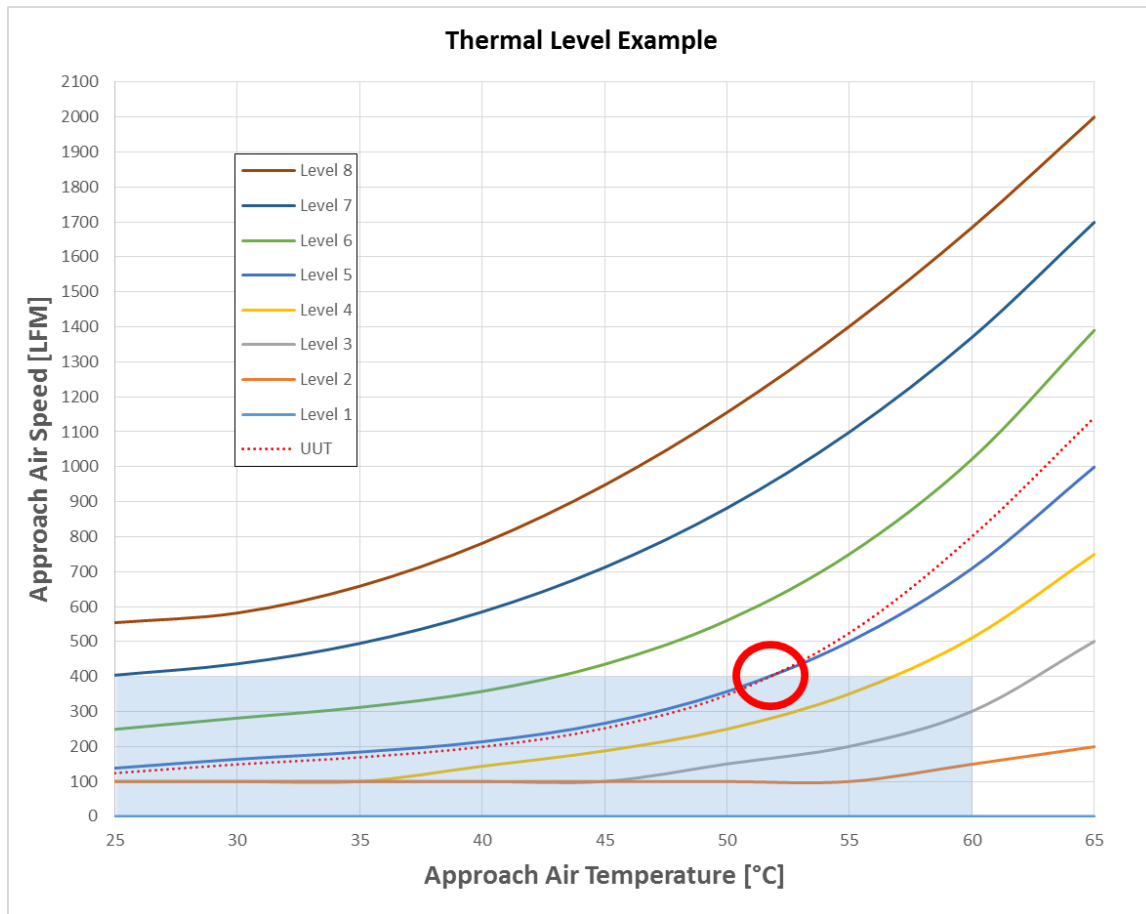


Figure 12-3. Example Add-in Card Thermal Profile

Table 12-2. Thermal Level Equations

Thermal Level	Equation (X=approach air temperature [Celsius]; Y= approach airflow speed [LFM])
0	Reserved
1	$Y = 0$
2*	$Y = -0.00093 * X^3 + 0.16705 * X^2 - 250.92807$
3*	$Y = 0.06667 * X^3 - 10.0000 * X^2 + 508.33333 * X - 8600.00000$
4*	$Y = 0.02700 * X^3 - 3.27605 * X^2 + 140.74670 * X - 1972.30735$
5	$Y = 0.01915 * X^3 - 1.82974 * X^2 + 62.21147 * X - 572.75974$
6	$Y = 0.02201 * X^3 - 2.00909 * X^2 + 66.82862 * X - 509.54545$
7	$Y = 0.00717 * X^3 - 0.11926 * X^2 - 3.31674 * X + 449.64286$
8	$Y = -0.00340 * X^3 + 1.28248 * X^2 - 57.26411 * X + 1237.37229$
9-15	Reserved

Note: * Approach air speed values for indicated Thermal Levels shall not be less than 100 LFM.

12.3. Degraded Thermal (DTherm) Level

The intent of the Degraded Thermal (DTherm) Level information is to determine the minimum airflow required at a given air temperature for which an Add-in Card, when provided the same stress application as it was for MaxTherm, will operate within its component's reliability limits but at a degraded Add-in Card performance level. Typically, this is accomplished by the Add-in Card's self-initiated thermal protection schemes, such as throttling. This is potentially of interest for platforms unable to provide sufficient cooling, such as due to the loss of a cooling fan which reduces the platform's cooling capacity. The reduced cooling capacity in such a case may be below the adapter's MaxTherm Level.

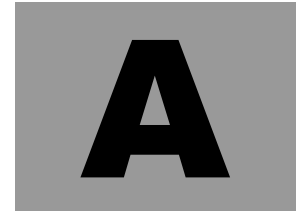
If an Add-in Card can operate at a reduced performance level to protect itself thermally and this translates into a reduced Adapter Thermal Profile then that established for MaxTherm, then DTherm is not equal to MaxTherm. DTherm is calculated using the same curves and process as MaxTherm, however, the Add-in Card's profile is created using the Add-in Card's most reduced performance operating level at which it is still on and providing useful work that is not less than 10% of its maximum sustained performance noted in MaxTherm testing. The DTherm field is defined for a value of 1 through 8 (inclusive). All other values are Reserved. Platform software must treat a Reserved DTherm value as if the Add-in Card is not capable of operating at a reduced performance level (i.e., platform software must use only MaxTherm value).

12.4. MaxAmbient

Some Add-in Cards may not be thermally viable up to an approach air temperature of 65 °C, regardless of the air speed involved. Or, even if the Add-in Card could be thermally viable at high temperature extremes, the airflow requirements to do so may require it to operate at a higher thermal challenge level, potentially reducing the number of systems able to supply the needed airflow. In either circumstance, the Add-in Card may opt to have its upper approach air temperature limit be less than 65 °C. This approach air temperature upper threshold is referred to as MaxAmbient. If MaxAmbient reporting is supported, the MaxAmbient field must contain a value between 32h (50 °C) and 41h (65 °C) inclusive. The number represents a temperature in degrees Celsius and is entered as a whole number. It applies to the full operating potential MaxTherm condition.

For the example of establishing a MaxTherm Level for an Add-in Card, as previously illustrated in Figure 12-2, if it was desired by the Add-in Card's developer to report less than a MaxTherm Level of 6, then a MaxAmbient value of 34h (representing 52 °C) could have been used by the Add-in Card's developer instead of 41h (representing 65 °C). In such a case, declaring a MaxTherm Level of 5 with a MaxAmbient of 34h would have been acceptable. If MaxAmbient is unsupported, then these bits must be set to 00h. Platform software must treat a Reserved MaxAmbient value as if MaxAmbient reporting was not supported (i.e., MaxTherm value applies up to 65 °C).

Appendix C describes the thermal test set up and procedure to evaluate an Add-in Card's thermal performance.



Appendix A. Insertion Loss Values (Voltage Transfer Function) (Informational Only)

The maximum loss values in dB (decibels) are specified for the system board and the Add-in Card. The insertion loss values are defined as the ratio of the voltage at the ASIC package pin (Transmitter/Receiver) and the voltage at the PCI Express connector interface, terminated by 100 Ω differential termination, realized as two 50 Ω resistances. These resistances are referenced to ground at the interface (see Figure A-1).

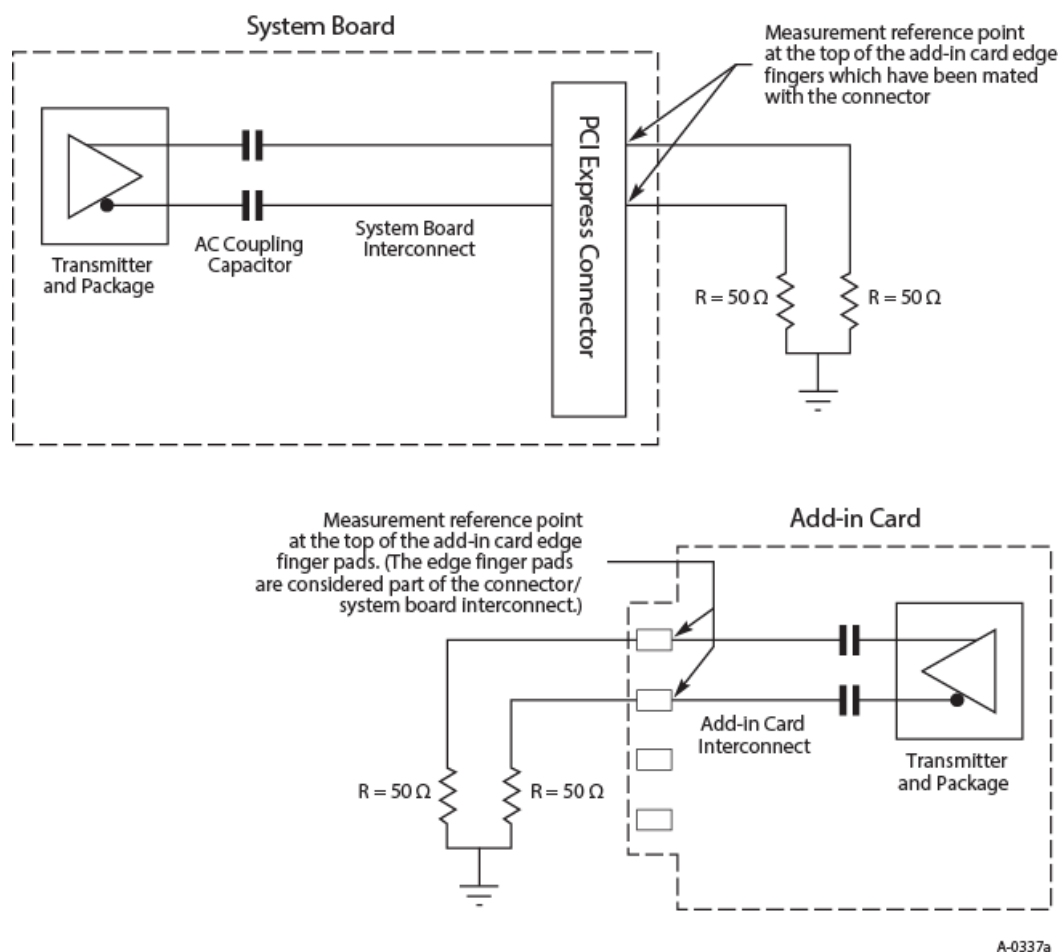


Figure A-1 Example Interconnect Terminated at the Connector Interface

All PCI Express differential trace pairs are required to be referenced to the ground plane (see Figure A-2). The loss values associated with any riser card interface and adjoining connector implementation must collectively meet the system board loss budget allocations and associated eye diagrams (see Table A-12-3).

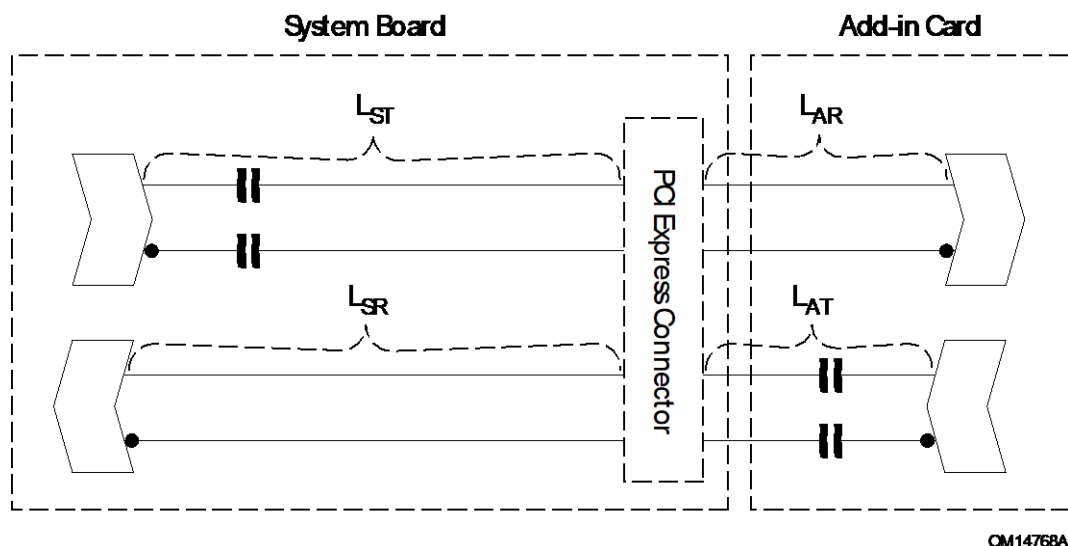


Figure A-2. Insertion Loss Budgets

Table A-12-3: Allocation of Interconnect Path Insertion Loss Budget for 2.5 GT/s Signaling

Loss Parameter	Loss Budget Value at 1.25 GHz (dB)		Loss Budget Value at 625 MHz (dB)		Comments
PCI Express Add-in Card	$L_{AR} < 2.65$	$L_{AT} < 3.84$	$L_{AR} < 1.95$	$L_{AT} < 2.94$	Notes 1, 2
System Board and Connector	$L_{ST} < 9.30$	$L_{SR} < 8.11$	$L_{ST} < 6.00$	$L_{SR} < 5.01$	Notes 1, 3
Guard Band	1.25		1.25		Note 1
Total Loss	$L_T < 13.2$		$L_T < 9.2$		Note 1

Notes:

1. All values are referenced to 100 Ω , realized as two 50 Ω resistances. The loss budget values include all possible crosstalk impacts (near-end and far-end) and potential mismatch of the actual interconnect with respect to the 100 Ω reference load.
2. The *PCI Express Base Specification* allows an interconnect loss of 13.2 dB for 1.25 GHz (non de-emphasized) signals and 9.2 dB for 625 MHz (de-emphasized) signals. From this, a total of 1.25 dB is held in reserve as guard band to allow for any additional attenuation that might occur when the Add-in Card and system board are mated. The allocated loss budget values in the table directly correlate to the eye diagram voltages in Section 4.8. Tradeoffs in terms of attenuation, crosstalk, and mismatch can be made within the budget allocations specified.
3. As a guide for design and simulation, the following derivation of the budgets may be assumed for 1.25 GHz signals: 5.2 dB is subtracted from 13.2 dB to account for near-end crosstalk and impedance mismatches. Out of this, the 1.25 dB is reserved as guard band. The following loss allocations are then assumed per differential pair: $L_{AR} = 1.4$ dB; $L_{AT} = 1.8$ dB; $L_{SR} = 6.2$ dB; $L_{ST} = 6.6$ dB. These allocation assumptions must also include any effects of far-end crosstalk. 625 MHz values may be derived in a similar manner.

4. The Add-in Card budget does not include the Add-in Card edge-finger or connector. However, it does include potential AC coupling capacitor attenuation on the Transmitter (TX) interconnect on the Add-in Card. The budget allocations generally allow for a maximum of 4-inch trace lengths for differential pairs having an approximate 5-mil trace width. No specific trace geometry, however, is explicitly defined in this specification. The subscripts of the symbol designators, T and R, represent the Transmitter and Receiver respectively.
5. The system board budget includes the PCI Express connector and assumes it is mated with the card edge-finger. Refer to Section 6.3 for specifics on the standalone connector budget. The system board budget includes potential AC coupling capacitor attenuation on the Transmitter (TX) interconnect on the system board. The subscripts of the symbol designators, T and R, represent the Transmitter and Receiver respectively.



IMPLEMENTATION NOTE

Insertion Loss Budget

The insertion loss budget distributions above are used to derive the eye diagram heights as described in Section 4.8. However, they are provided here only as a design guideline. Compliance measurements must actually be verified against the eye diagrams themselves as defined in Section 4.8.

Appendix B. Test Channel Scattering Parameters

B.1. 8.0 GT/s Test Channels

The 12-port S-parameter for the System-Board Test Channel with and without a standard connector/edge-finger model are distributed with this specification in the following files:

- `system_board_test_channel_with_connector_8 G.s12p`
- `system_board_test_channel_without_connector_8 G.s12p`

The 12-port S-parameter for the Add-in Card Test Channel with and without a standard connector/edge-finger model are distributed with this specification in the following file:

- `add_in_card_test_channel_with_connector.s12p`

B.2. 16.0 GT/s Test Channels

The 12-port S-parameter for the System-Board Test Channel with connector/edge-finger model are distributed with this specification in the following files:

- `system_board_test_channel_with_connector_16G.s12p`

The 12-port S-parameter for the Add-in Card Test Channel without a standard connector/edge-finger model are distributed with this specification in the following file:

- `Add_in_Card_test_channel_with_connector.s12p`

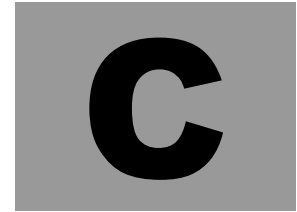
B.3. 32.0 GT/s Test Channels

The 4-port S-parameter for the System-Board Test Channel with connector/edge-finger model are distributed with this specification in the following files:

- `System_board_test_channel_withpkg.s4p`

The 4-port S-parameter for the Add-in Card Test Channel without a standard connector/edge-finger model are distributed with this specification in the following file:

- `Add_in_Card_test_channel_withpkg.s4p`



Appendix C. Thermal Data Collection and Test Procedure

This appendix describes the thermal test set-up and procedure to evaluate an Add-in Card's thermal performance. Thermal performance is communicated via the following four VPD fields:

- AFI Level
- MaxTherm Level
- DTherm Level
- MaxAmbient

The values of these fields are determined using a custom test fixture. Details regarding the dimensions and construction of the test fixture are provided in the associated CAD files (refer to the PCI-SIG website) for the thermal challenge and airflow impedance tester.

The test fixture is intended to be attached to an AMCA 210-99/ASHRAE 51-1999 compliant airflow chamber, which can quantify both static pressure as well as volumetric airflow. The tester is attached to the airflow chamber such that air blows toward the PCIe Add-in Card and exits the tester at the Add-in Card's I/O bracket.

For MaxTherm and DTherm level testing, the airflow impedance plates (shown as orange in color in Figure C-1) must be removed. For AFI Level testing, where the desire is to understand the relative airflow impedance of the Add-in Card, the use of the airflow impedance plates (two when testing SINGLE-SLOT Add-in Cards; one when testing DUAL-SLOT Add-in Cards) is required.

The Add-in Card to be tested is installed in the test fixture, which is positioned above an operational platform's PCIe connector. Any cables needed to fully exercise the Add-in Card are attached to the Add-in Card to be tested. The test fixture's lid is then attached, and the test fixture is checked to ensure air flow is not leaking through its joints.

The Add-in Card is operated to its rated TDP level using a vendor-specific exercise procedure. The Add-in Card's manufacturer is responsible for providing sufficient detail - including full descriptions of all software, firmware, and hardware needed, such that others could recreate the same results if provided the same Add-in Card.

See the associated CAD file information for details of the tester's construction and size. Figure C-1 shows an exploded view of the tester, with the lid, its mounting screws, the AFI blocks (shown in orange for illustration purposes only), and Add-in Card under test (in green) shown suspended above the tester housing.

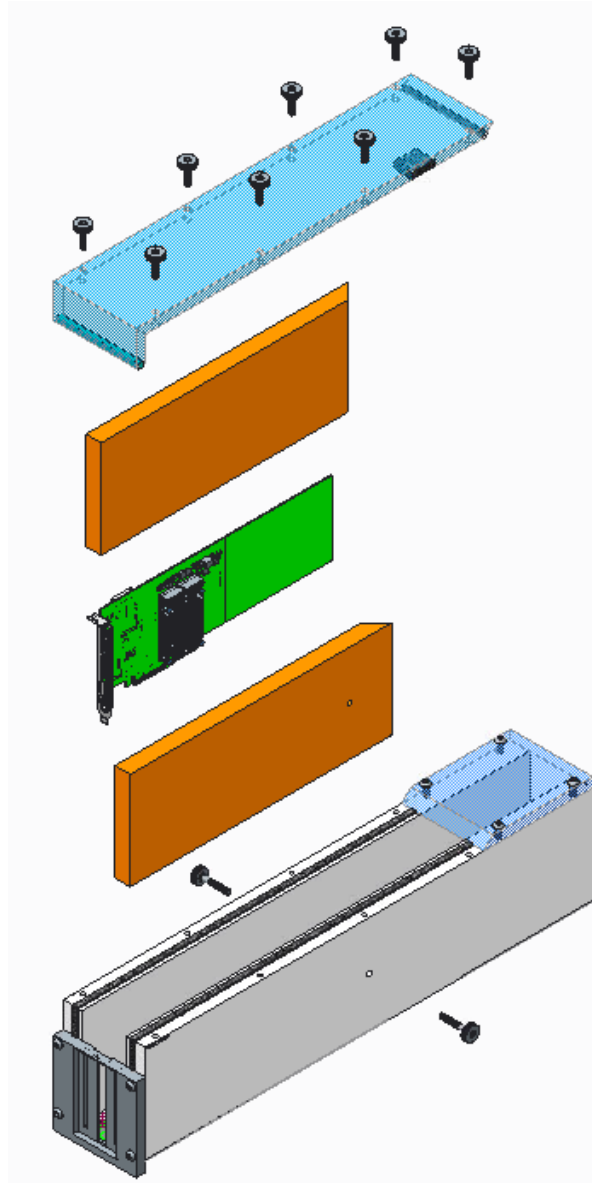


Figure C-1. Tester isometric exploded view: {Lid, AFI Block, Add-in Card, AFI Block}

During Thermal Level testing for MaxTherm and DTherm data, the AFI blocks (shown in orange in Figure C-1) are not used in the tester as shown in Figure C-2. The tester is connected to a flow bench which provides quantifiable volumetric airflow and static pressure.

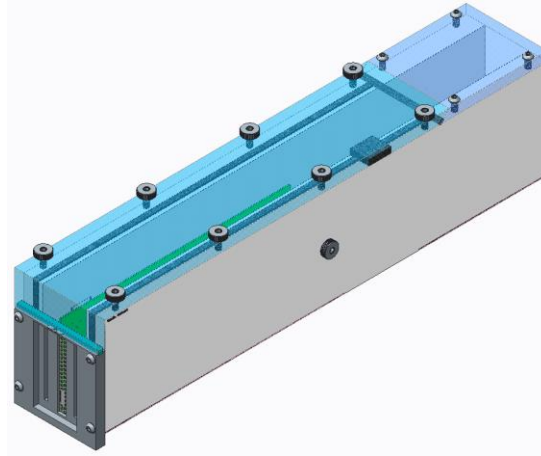


Figure C-2. Tester isometric view in MaxTherm and DTherm Testing Configuration

During Thermal Level testing for AFI Level data, the AFI blocks (shown in orange in Figure C-1) are used in the tester (two AFI blocks when testing SINGLE-SLOT Add-in Cards as shown in Figure C-3 one AFI block when testing DUAL-SLOT Add-in Cards as shown in Figure 12-2).

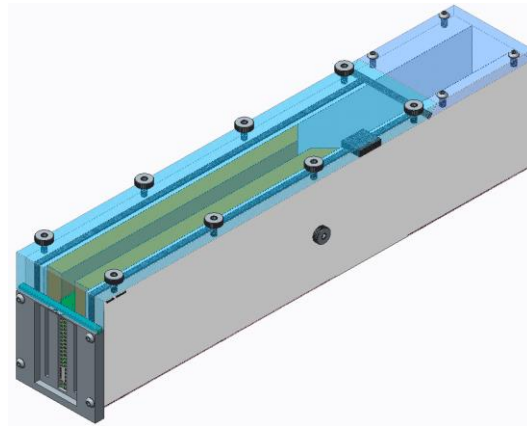


Figure C-3. Tester isometric view in SINGLE-SLOT Add-in Card AFI testing configuration

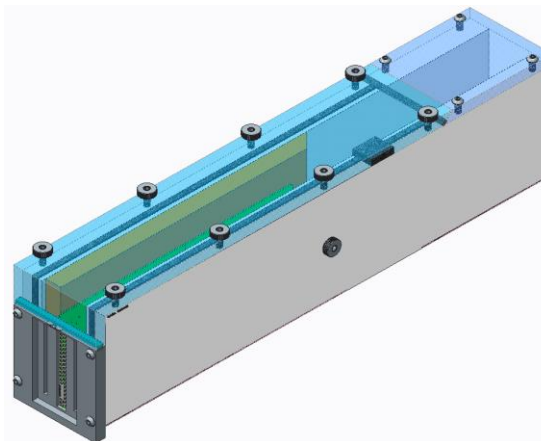
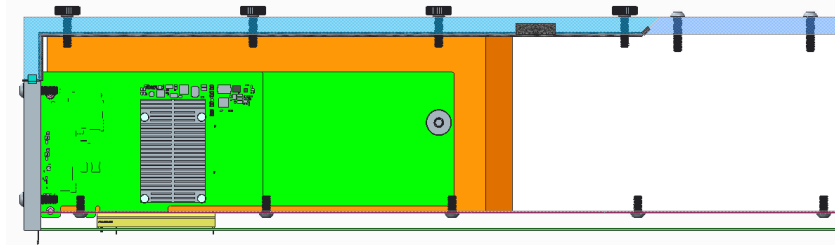


Figure C-4. Tester isometric view in DUAL-SLOT Add-in Card AFI Testing Configuration



**Figure C-5. Side view in DUAL-SLOT Add-in Card AFI Testing Configuration
(Side wall removed for viewing illustration only)**

A system board with at least one x16 PCIe slot capable of operating at the Add-in Card's maximum link width and maximum link speed is needed for the testing. The PCIe slot must be able to send a Set_Slot_Power_Limit Message value that allows the Add-in Card to operate at its higher performance level. The platform power supply must be able to supply the power required for both the system board and the Add-in Card to run at their highest performance levels, including any additional Add-in Card power cables (if used).

For MaxTherm and DTherm testing, the quantified volumetric airflow is divided by the cross-sectional area of the duct to establish the average velocity of air entering the test fixture:

velocity (ft/min) = volume flow (ft³/min) / tester's inner area (ft²) perpendicular to airflow.

Hot-wire anemometer must be placed at the center of tester's air channel, within 50 mm downstream of the tester's air entrance opening. The anemometer data must be collected for reference only. At least one thermocouple sensor is required to be placed at this same location to collect inlet air temperature data, unless also using the anemometer's local ambient temperature reading. Figure C-6 shows an example test setup connected to a flow bench.



Figure C-6. Actual Thermal Level Test Fixture Set-up

The target output is the air speed (LFM, or FT / min) required to cool the Add-in Card under test at projected (or actual) air temperatures while the Add-in Card is being stressed to its TDP level. The Add-in Card component's minimum temperature margin at various air speeds are collected, while also noting the air temperature entering the test fixture. The Add-in Card's minimum temperature margin is added to

the tester's air inlet temperature to arrive at a projection as to what would be the zero-temperature margin ambient for given air speeds. With the exception of Add-in Cards meeting the requirements of Thermal Level 1, no fewer than six data points, regularly spaced from a project approach ambient of 25 °C to at least 50 °C (65 °C preferred), are to be collected. These projected approach ambients and approach air speeds are then compared against the Thermal Levels shown in Figure 12-2.

For example, a hypothetical Add-in Card was profiled for its thermal levels using an airflow chamber, such as the one shown in Figure C-7, at various air speeds.

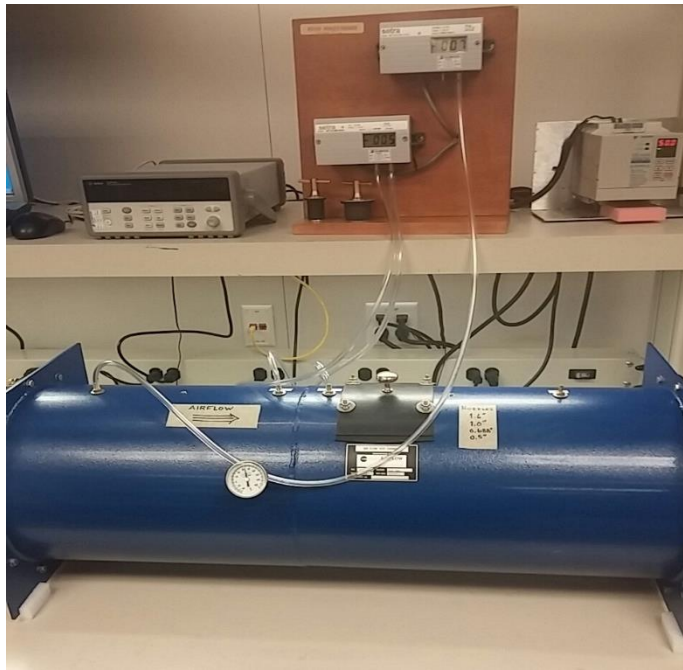


Figure C-7. An Example of an Airflow Chamber

Several measurement points are made to enable a good curve fit across the range of interest. The components with the least temperature margin are monitored using either temperature sensors that are part of the Add-in Card's design or added thermocouples. An optical transceiver plug, technically not a part of the Add-in Card, but being integral for its intended usage, is included in this Add-in Card's characterization. The results for this example Add-in Card are given in Table C-1.

Table C-1. Hypothetical Fabric Add-in Card Thermal Level Measurements

	Test Run								
	1	2	3	4	5	6	7	8	9
Approach Ambient Temperature (°C)	26	26	26	26	25	25	25	25	25
Measured CFM	49	41	32	27	23	18.5	15	12	7.5
VR Temperature (thermocouple reading: 100 max allowed) (°C)	39.3	40	41	42	44	47	56	65	76
QSFP Temperature (Add-in Card sensor reading: 70 max allowed) (°C)	31	34	38	41	43	47	52	56	68
ASIC Temperature (Add-in Card sensor reading: 105 max allowed) (°C)	54.5	55	56	58	60	64	78	92	105

From these measurements the average air speed in LFM (linear feet per minute) can be calculated by dividing the volumetric airflow in CFM (cubic feet per minute) by the tester's inner channel area. The tester's inner dimensions are 4.724 inches in height by 2.337 inches in width. Table C-2 shows the results of the calculated LFM.

Table C-2. Hypothetical Fabric Add-in Card's Calculated Approach LFM

	Test Run								
	1	2	3	4	5	6	7	8	9
Approach Ambient Temperature (°C)	26	26	26	26	25	25	25	25	25
Measured CFM	49	41	32	27	23	18.5	15	12	7.5
Tester's inner channel height (IN)	4.724	4.724	4.724	4.724	4.724	4.724	4.724	4.724	4.724
Tester's inner channel width (IN)	2.337	2.337	2.337	2.337	2.337	2.337	2.337	2.337	2.337
Calculated LFM (CFM/tester's channel area)	639.1	534.8	417.4	352.2	300.0	241.3	195.7	156.6	97.8

The temperature margins at the different air speeds measured are calculated by subtracting the measured temperature for each component from its maximum allowed temperature for reliability and data integrity, sometimes referred to as the component's maximum continuous operating temperature, or MCOT. No additional temperature margin or safety factor must be used in these calculations.

By adding the test run's actual measured approach ambient to the least temperature margin for the Add-in Card's components, the result is the maximum approach ambient supportable for that air speed. Note in this example, how under different air speeds, different components may have the least temperature margin for the Add-in Card.

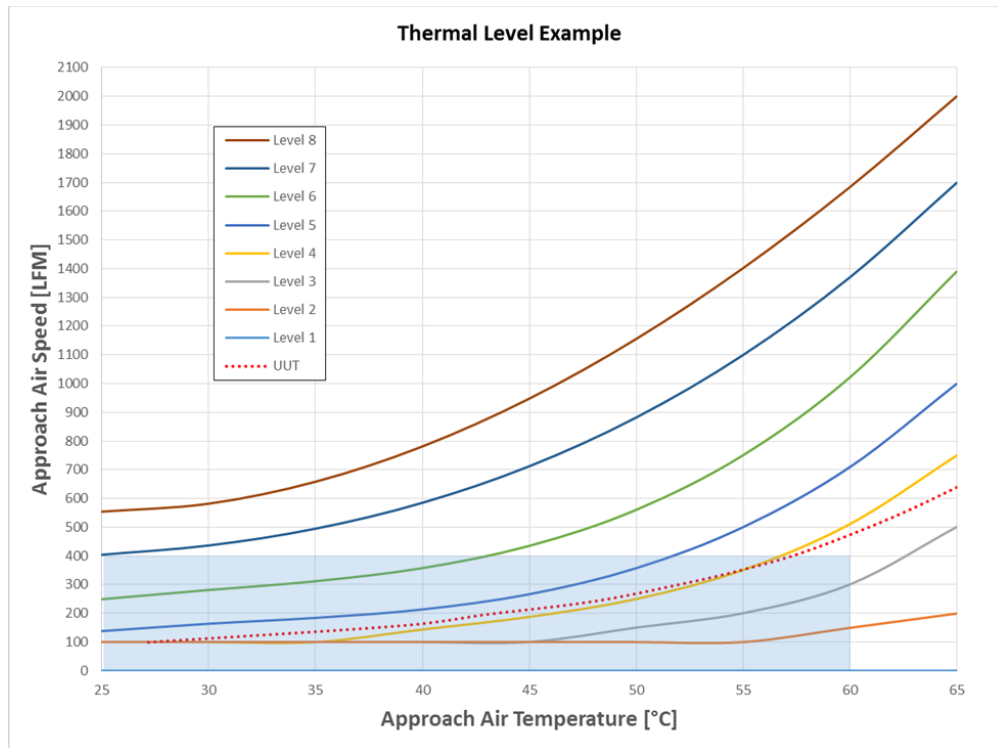
Following the steps discussed, the approach temperature to plot against the calculated LFM for this example Add-in Card may be determined, as shown in Table C-3.

Table C-3. Example Fabric Add-in Card's Calculated Approach Air Temperature

	Test Run								
	1	2	3	4	5	6	7	8	9
Approach Ambient Temperature (°C)	26	26	26	26	25	25	25	25	25
VR margin to 100 °C (°C)	50.7	50	49	48	46	43	34	25	14
QSFP margin to 70 °C (°C)	39	36	32	29	27	23	18	14	2
ASIC margin to 105 °C (°C)	50.5	50	49	47	45	41	27	13	0
Max Approach Temperature at Calculated LFM [Approach Ambient + Least Margin Component] (°C)	65	62	58	55	52	48	43	38	25

Plotting the resulting max approach level against the calculated LFM graphically displays how the Add-in Card compares to the various Thermal Levels, as shown in Figure C-8.

Note that this Add-in Card's plot never exceeds Thermal Level 5. Even though it is under Thermal Level 4 when above approach air temperatures of approximately 57 °C, its MaxTherm Level would be 5 (to cover the mandatory range below 50 °C. Since it could operate up through an approach air temperature of 65 °C, it would specify a MaxAmbient value of 41h. Using a lower MaxAmbient value would not allow this Add-in Card the advantage of using a lower Thermal Level, so it must declare the maximum ambient it could support, up to the limit of 65 °C.

**Figure C-8. Example Add-in Card's Thermal Level**

Since this example Add-in Card does not support lowered power levels/lowered performance when under adverse environments, its DTherm Level is the same as its MaxTherm Level.



Appendix D. Thermal Management

D.1. 10 W/25 W/75 W/150 W Thermal Characterization

To ensure robust system operation and reliability, Add-in Cards should undergo thermal characterization (see Figure D-4). The following guidelines should be used when performing thermal characterization for Add-in Cards up to 150 W that do not support Thermal Reporting Vital Product Data. If dynamic system cooling response or detailed information for thermal operation or flow impedance is desired, Thermal Reporting Vital Product Data and associated testing should be utilized.

- The design of the test system or fixture, including appropriate slot airflow, is left to the discretion of the Add-in Card vendor.
- The Add-in Card should be operated to its rated TDP level using a vendor-specific exercise procedure.
- The test should be performed in a thermal chamber such that the card's ambient temperature is brought to the card's rated operational temperature and with an empty slot or equivalent empty space on each side of the card.

For Add-in Cards with an integrated air mover:

- Ambient temperature is defined as the average air temperature at the fan inlet. Since the fan location may vary for different cards, should the exact number and location of the inlet temperature measurements is left to the discretion of the Add-in Card vendor.
- Any airflow characteristics exiting the rear I/O bracket is of great interest and value to system builders. When requested, card vendors should work with system builders to define how to measure those characteristics.

For Add-in Cards without an integrated air mover:

- Ambient temperature is defined as the average air temperature 25 mm (1.0 inches) upstream of the leading edge of the card. This corresponds to the location of incoming air over the card in a typical ATX-based system.
- Card airflow should be recorded in the same location as the temperature measurement for thermal characterization and should be reported alongside temperature ratings in LFM. For example, thermal characterization performed in a system or fixture with 600 LFM of airflow over the slot may yield substantially different results than the same test with 50 LFM over the slot. The LFM that was used when qualifying a card to a rated temperature is valuable information for system integration.

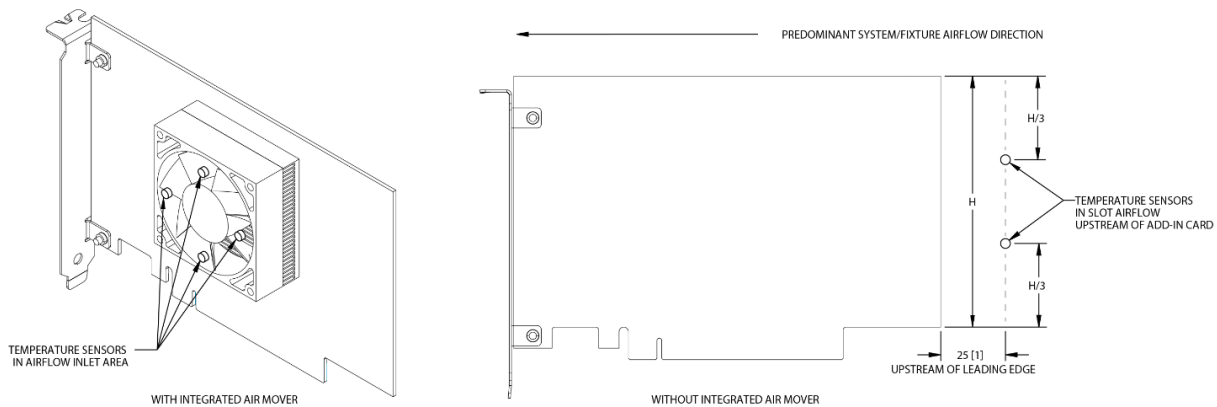


Figure D-4. Thermal Characterization

D.2. 150 W Thermal Management

Increasing power has a corresponding impact on the thermal management solutions of both the PCI Express 150 W Add-in Card and the platforms that support them. To guarantee robust system operation and reliability, the card and system should work together to dissipate the additional thermal load the 150 W Add-in Card puts on the system. It is recommended that the card manage its exhaust flow with respect to the system enclosure. For most ATX systems, it is recommended that the card exhaust heat to the outside of the system enclosure. This type of card thermal solution has the least impact on systems that use typical ATX chassis designs.

For other 150 W Add-in Card thermal designs, it is recommended that the card manufacturer and chassis designer or system integrator work closely together to ensure the card, chassis, and system components work together so that performance and component reliability are not impacted.

D.3. PCI Express 225 W/300 W Add-in Card Thermal and Acoustic Management

Increasing card power has a corresponding impact on the thermal (for example, inlet temperature and airflow) and acoustic management solutions of the PCI Express 225 W/300 W Add-in Cards and the platforms that support them. To ensure robust system operation and reliability, the high-power cards and systems should work together to dissipate the additional thermal load the card puts on the system.

D.3.1. Inlet Temperature

Inlet temperature is defined as the average temperature at the card thermal solution's fan inlet. Since the fan location may vary for different cards, the exact locations for the inlet temperature sensors placement is left to the discretion of the Add-in Card vendor. Figure D-5 illustrates an example showing the temperature sensor placement at the thermal solution inlet; one may consider the average temperature measured by the different sensors as the inlet temperature.

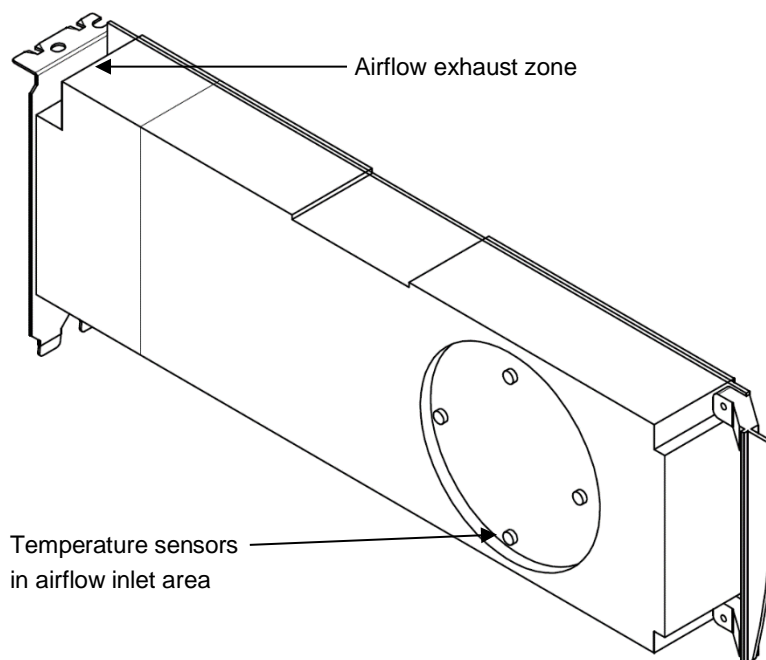


Figure D-5: Example of High-Power Card Showing Temperature Sensor Placements at the Thermal Solution Inlet

The procedure described in Section D.3.2 should be used as a guideline for characterizing the high-power Add-in Card. The Add-in Card inlet temperature should be controlled at 45 °C for both 300 W and 225 W cards.

For Add-in Cards with a forced convection thermal solution, the rear bracket should include vents for airflow exhaust to the outside of the system. Any airflow exhaust inside the system should be located at the rear end of the Add-in Cards as shown in Figure D-5. It is recommended that any airflow exhaust inside the system be located within 2.0 inches of the rear bracket.

D.3.2. Card Thermal Characterization Procedure

The following method should be used to carry out thermal characterization of any 225 W/300 W Add-in Card:

The measurement should be carried out on a 225 W/300 W Add-in Card with an open bench test setup system as shown in Figure D-6 to Figure D-8. Figure D-6 illustrates a setup to test a DUAL-SLOT card. Dimensions in Figure D-6 apply to other fixture versions shown in Figure D-7 and Figure D-8 except where indicated otherwise. The fixture may be made of ¼ inch thick polycarbonate plastics, simulating adjacent full-length cards and a standard rear chassis panel.

Use the following test procedure:

1. Install the card under test in one of the test setups or fixtures shown in Figure D-6 to Figure D-8 according to the card volumetrics.
2. Place the test setup in a thermal chamber and adjust the chamber temperature such that the card's inlet temperature is 45 °C (for both 300 W and 225 W cards).
3. Each of the applicable thermal characteristic measurements listed below should be carried out with the card in idle and full power states. The “idle” and “full power” states are defined by the Add-in Card vendor and are to be recorded as the condition under which the thermal characterization is performed.
 - Critical component temperatures
 - Critical temperature limits
 - Inlet temperature
 - Exhaust temperature
 - Fan speed

Airflow (CFM) values exiting the rear I/O bracket is important to system builders. When requested, card vendors should work directly with system builders on the details of how to measure the CFM.

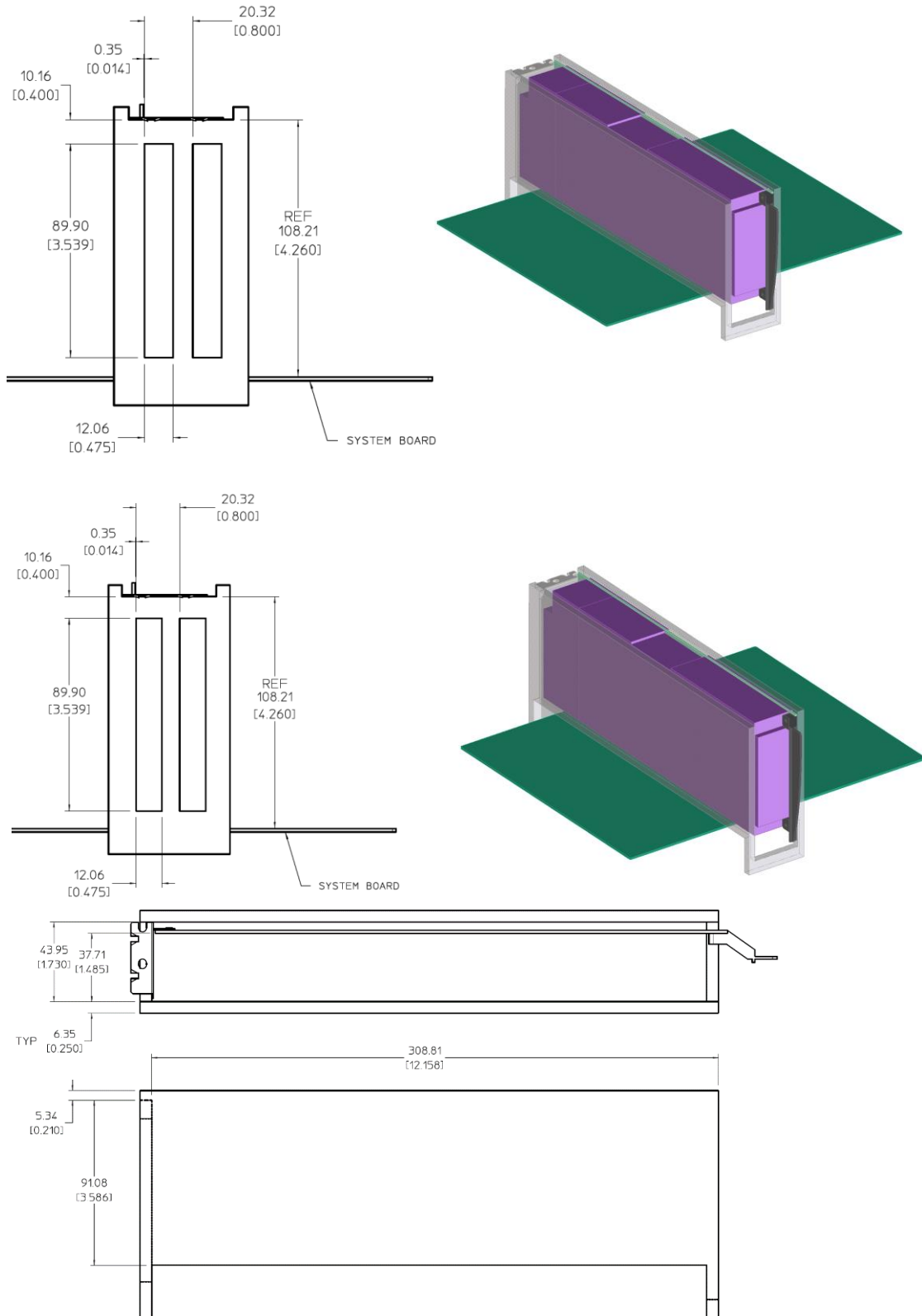


Figure D-6: Thermal Characterization Fixture – DUAL-SLOT Add-in Card Version

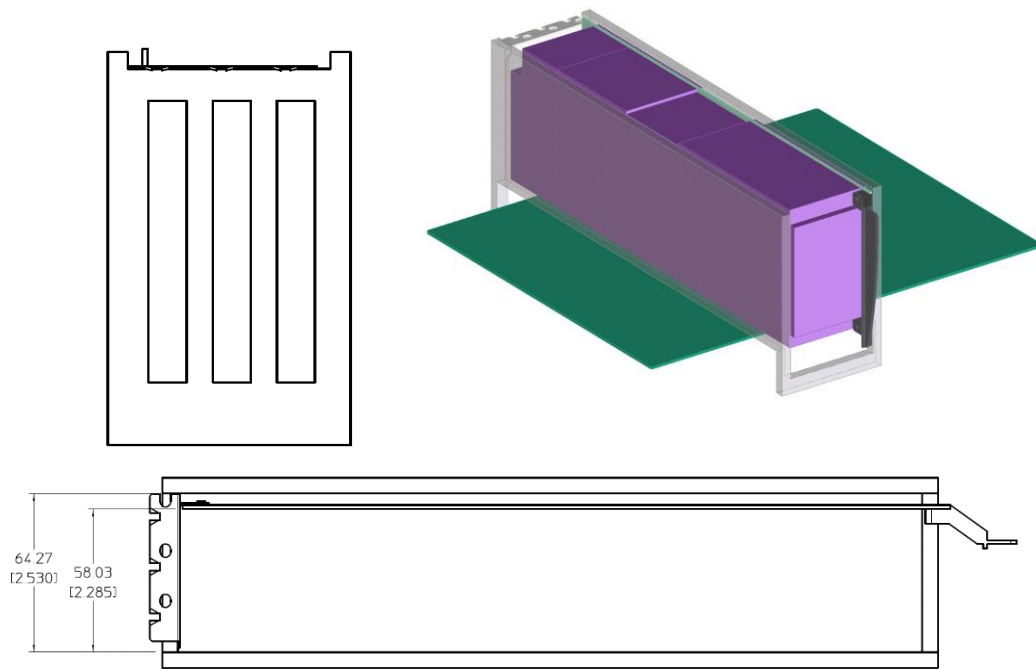


Figure D-7: Thermal Characterization Fixture – TRIPLE-SLOT Add-in Card Version

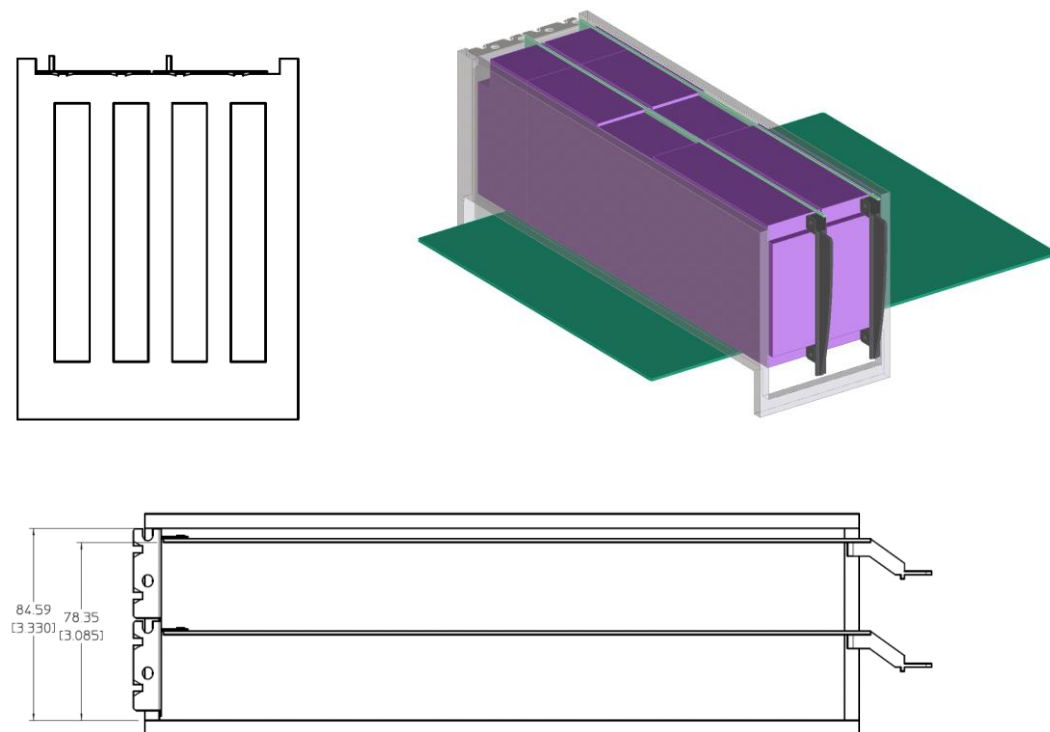


Figure D-8: Thermal Characterization Fixture – Tandem DUAL-SLOT Version

D.3.3. Acoustic Management

The acoustic emission of a system is increasingly important for computer systems. This is becoming more challenging with higher power systems. The acoustic noise sources in a system are typically the cooling fans, the power supply fan, the graphics card fan, the hard drive, and the optical drives.

The high-power card manufacturers, the chassis designers, and the system integrators should work closely together to deliver a reasonable solution, such that the end user experience is not impacted.

D.3.3.1 Background and Scope

The acoustic noise generated by high power PCI Express cards can be a significant contributor to overall system noise and, in fact, can be the loudest single component in the computer system. Card and system vendors should work together to make sure the acoustic emissions meet end-user requirements, contractual requirements, and/or government-mandated acoustic standards.

This specification does not define acoustic requirements for card compliance. Instead, this specification lists general guidelines and defines a method for measuring card acoustics. This method is intended to help system and card vendors to understand acoustic performance of the cards and to work together more efficiently and reduce acoustic emissions.

D.3.3.2 Acoustic Characterization Procedure for Add-in Card with Integrated Air Mover

The following method uses an industry-standard method, ISO 3744, to measure acoustic emissions and adapts it to the constraints associated with Add-in Cards that have at least one fan. This method uses the “idle” and “full power” fan speed data gathered in the Card Thermal Characterization Procedure (see Section D.3.2).

1. Measurement and test setup should be as defined in ISO 3744, Acoustics – Determination of Sound Power Levels of Noise Sources Using Sound Pressure – Engineering Method in an Essentially Free Field Over a Reflecting Plane.
2. Place the card in the acoustic chamber by itself, in free air, without the system board or any other system components. The card under test must be suspended by some type of “bungee cords” to avoid any fixturing effect on acoustics. The detailed implementation of the “bungee cords” is up to each card manufacturer.
3. It is not necessary to fully power or operate the card. Instead, it is necessary to operate only the Add-in Card’s fan(s); this can be accomplished with an external power source and fan control circuit.
4. Measure and/or calculate the following acoustic emissions at both the “idle” and “full power” fan speeds.
 - Sound pressure, L_{PA}
 - Sound power, L_{WA}
 - 1/3-octave acoustic spectral content



IMPLEMENTATION NOTE

Acoustic Characterization

Any equipment used for fan power and control must be located outside the acoustic chamber or be sufficiently quiet so as not to contribute to the acoustic measurements.

The particular circuit (i.e., waveform) used to control the fan may have a significant effect on the acoustic results, especially at low fan speeds.

D.3.3.3 Acoustic Recommendations and Guidelines

In addition to minimizing the overall acoustic levels, the following points should be considered:

- The acoustic emissions should not include any prominent tones.
- Certain frequencies are more objectionable to humans than others.
- The Add-in Card's fan(s) should be dynamically controlled to minimize noise over the complete range of expected operational and environmental conditions.
- The Add-in Card's fan(s) should be controlled such that there are no abrupt changes or noticeable oscillations in acoustic levels or quality.
- The chassis should be designed to minimize coupling of vibrations and acoustic noise from the Add-in Card to the chassis.
- The Add-in Card should be designed to minimize coupling of vibrations from the Add-in Card's fan to the Add-in Card.

D.4. Liquid Cooling Enablement

D.4.1. Thermal Transfer Plate

Add-in Cards that have high power consumption may benefit from a high-performance Add-in Card cooling method such as liquid cooling to serve as an alternative to conventional passive or fan-driven air cooling. One example implementation for mating of a liquid cooling assembly to an Add-in Card is a Thermal Transfer Plate (TTP). The function of the TTP is to conduct heat from Add-in Card components to a mating surface on which the liquid cooling assembly is attached. The liquid cooling assembly in turn carries heat away from the Add-in Card.

While it is generally recognized that liquid cooling may be needed at Add-in Card power levels beyond 450 W, no power thresholds requiring liquid cooling or TTP are provided in this specification. Liquid cooling may be chosen to reduce the volume consumed by conventional heatsink, fan, and air duct solutions, and add flexibility to component height and placement, for example. Further, systems that require liquid cooling for high power cards may also benefit from applying a liquid cooling assembly to other, lower power Add-in Cards to reduce the overall chassis air cooling burden. Chassis-level cooling guidance is beyond the scope of this specification. This appendix will focus on design considerations at the Add-in Card level.

The TTP is a structure that is installed in place of the heatsink, duct, and in some cases fan that would normally be used for air cooling of the Add-in Card. This plate serves as a thermally conductive interface between the Add-in Card PCB heat generating components and an attached liquid cooling assembly. The Add-in Card and TTP are designed to accept a liquid cooling assembly that is driven by a separate external or chassis-level pumping system. The example TTP described in this section has a defined bolt pattern and maximum overall thickness to help eliminate the additional design effort of producing a separate cold plate design for each product. This is intended to encourage reuse across various Add-in Cards.

The bottom surface of the TTP contacts PCB mounted components to transfer heat to its top surface for cooling via the attached liquid cooling assembly. Since the Add-in Card components' location, height, and heat generation will vary between designs, the mechanical profile of the component-facing (bottom) surface of the TTP may be customized to best accommodate the layout and cooling needs of those heat generating elements. The bottom face of the TTP typically contacts components on the Add-in Card through a compliant Thermal Interface Material (TIM) to ensure a conformal, continuous thermal path to the TTP. Depending on design, board components may be contacted/cooled by the TTP while others may be left components exposed. Exposed components might include power connectors, capacitors, or I/O connectors, for example.

Figure D-9 shows an exploded view of an Add-in Card with the TTP.

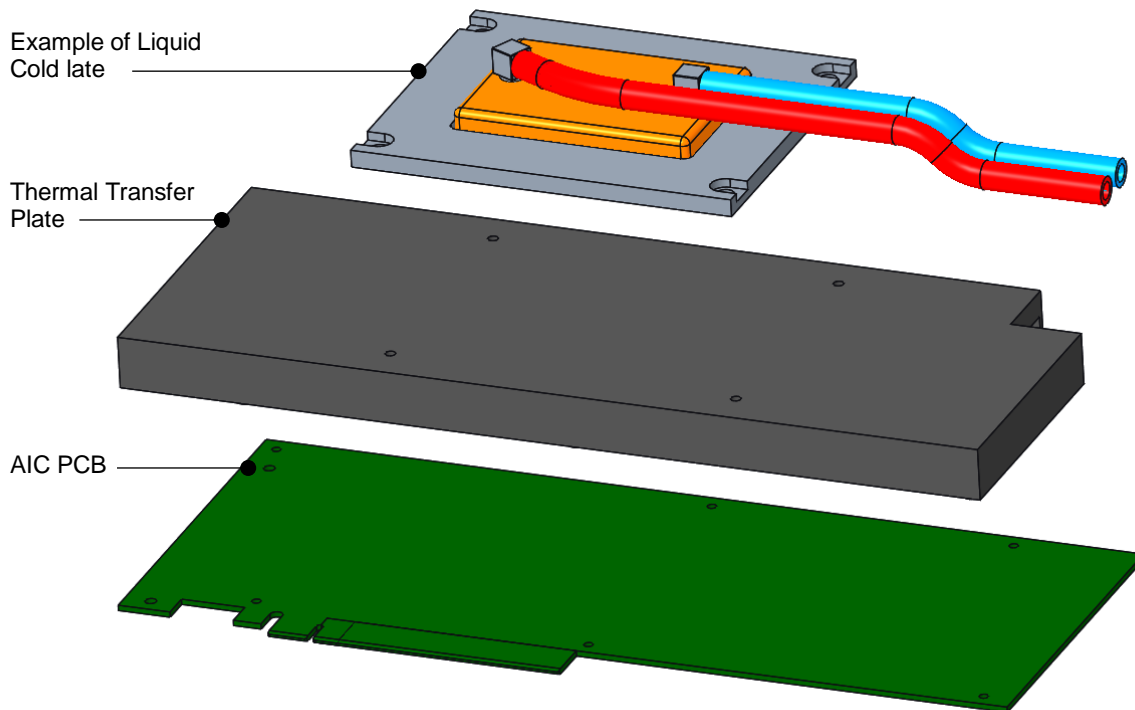


Figure D-9. Exploded View of Card with TTP

D.4.2. TTP Design Considerations

- The use of a TTP does not require or preclude use of supplemental air flow. However, the trend in liquid cooled systems is toward reduced airflow. Add-in Card designers should consider the scenario where the Add-in Card is only cooled by the mated liquid cooling assembly with no supplemental air flow.
- The range of thickness for the TTP allows for customization of the TTP based on the Add-in Card design.
- The top surface of the TTP provides an interface for mounting the liquid cooling assembly. Flatness of the top surface should be defined to ensure proper contact with the mating liquid cooling assembly.
- An example mounting hole pattern on the TTP for attachment of the liquid cooling assembly is shown. Such a mounting pattern allows system vendors to design a single liquid cooling assembly that may be used on a variety Add-in Card. However, Add-in Cards may require unique liquid cooling assemblies depending on their component temperature requirements or layout.
- The location of the mounting hole pattern may be adjusted as illustrated in Figure D-14.
- The TTP may include heat pipes, vapor chamber, or other thermal enhancement technologies to move heat more efficiently to the top surface of the TTP.
- The TTP may be designed with a cutout for the main heat generating chip to allow for direct contact of the liquid cooling assembly. This option allows for a reduced thermal resistance (and thus lower operating temperature) due to the removal of the plate spreading resistance and one layer of TIM material between the primary heat source and the liquid cooling assembly. Direct mating to the primary heat source will require a liquid cooling assembly that is more customized for its application. An example is illustrated in Figure D-10.

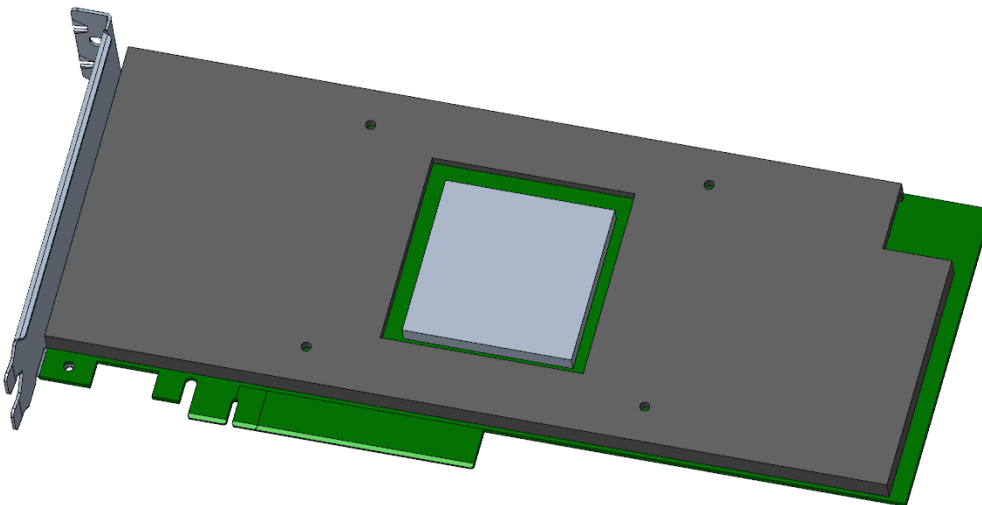


Figure D-10. View of Example TTP with Cutout for Primary ASIC

D.4.3. TTP Definition Guidelines

D.4.3.1 Supported Add-in Card Types

The TTP may be used for the following types of Add-in Cards:

- DUAL-SLOT Card
- TRIPLE-SLOT Card
- Half-length, Three-quarter-length, and Full-length Add-in Cards

Liquid cooling solutions for SINGLE-SLOT Add-in Cards may be possible but is not explored in this specification.

The TTP and the combined TTP and liquid cooling assembly should not violate the existing Add-in Card form factor keep-in boundaries. Any tubing for the cooling medium that lies within the perimeter of the Add-in Card should also remain within the primary side component volume.

The maximum thickness of the TTP (dimension H1) as defined in Table D-1 drives the remaining allowable space for the attached the liquid cooling assembly within the Dual Slot form factor. H1 is defined as a maximum to ensure that system designers have sufficient space available for liquid cooling assemblies.

Table D-1. Allowable Dimensions for TTP Height Cooling Solution

Dimension Name	Definition	Dimension
H1 (Maximum)	Height of TTP from top side of card (see Figure D-10 and Figure D-12)	15.5 mm REF
H2 (Minimum)	Thickness of spreader portion of TTP (see Figure D-12)	Not Specified
Minimum Topside Height Remaining for Liquid Cooling Assembly (Double Wide Cards)	[Topside Keep-in Double Wide] – H1	19.3 mm REF
Minimum Topside Height Remaining for Liquid Cooling Assembly (Triple Wide Cards)	[Topside Keep-in Triple Wide] – H1	39.62 mm REF

D.4.3.2 TTP Thickness

The TTP surface may fall below the maximum height (H1) but should maintain the standardized mounting hole pattern for the liquid cooling assembly.

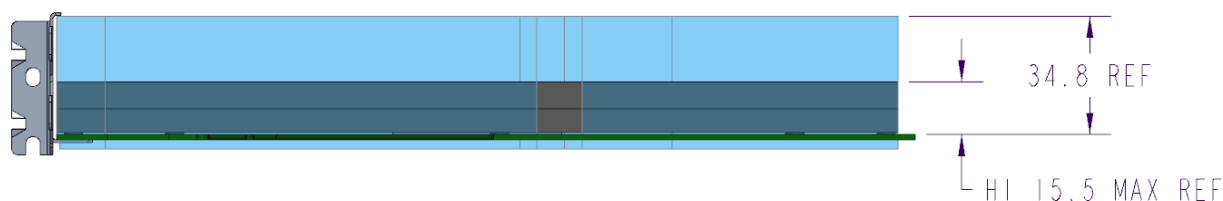
Vendor considerations for TTP height are:

- Existing and future Add-in Card designs
- Multi-chip Add-in Card designs
- Add-in Cards with optical transceivers (e.g. QSFP, SFP+)

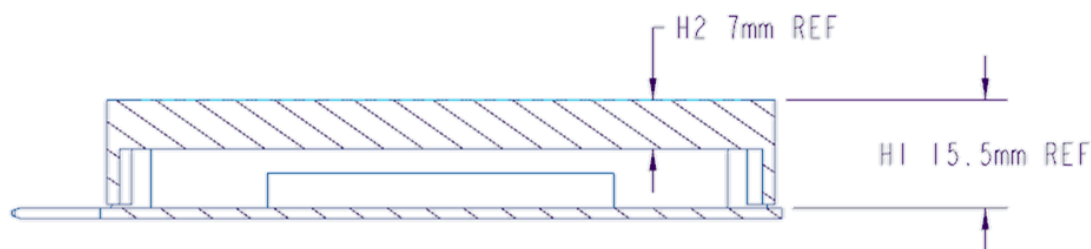
The TTP spreader thickness (H2) around the mounting holes should be controlled to a specific minimum dimension to ensure proper thread depth and number of threads needed to meet shock and vibration requirements. Outside the liquid cooling assembly mounting area H2 may be thinner or thicker as Add-in Card cooling needs dictate.

The bottom side of the TTP's mechanical profile may be designed accommodate the layout and cooling needs of the Add-in Card's heat generating elements. The bottom side of the TTP will typically contact components on the Add-in Card through compliant thermal interface materials. The Add-in Card vendor decides what board components will be contacted/cooled.

See Table D-1 for the key TTP dimensions.



**Figure D-11. Example Card Bottom View (from edge connector side)
DUAL-SLOT Add-in Card**



**Figure D-12. Section View Showing Example TTP Overall Thickness (H1) and
Spreader Thickness (H2)**

D.4.3.3 Liquid Supply and Return Routing

System designers may implement tube routing through East, West or North side depending on the Add-in Card design and the liquid cooling assembly design (see Figure D-13).

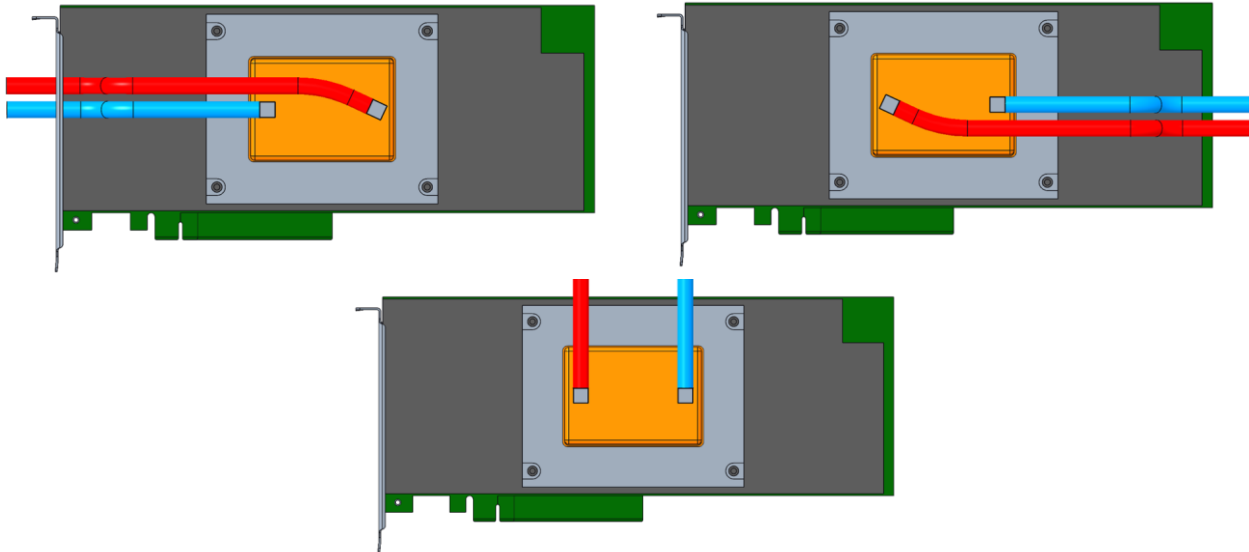


Figure D-13. Example Tube Routing Directions: West/East/North

D.4.3.4 Example Liquid Cooling Assembly Mounting Hole Locations

- An example mounting hole quantity (4x) and pattern is defined in Figure D-11 below – see dimensions X2 and Y2.
- The location of the mounting hole pattern may be adjusted within an example keep-in boundary as shown in Figure D-14. The boundary is defined by dimension B1 at the east and west edges of the Add-in Card and dimension B2 at the north and south edges of the Add-in Card. The mounting hole dimensions X2 and Y2 should be maintained within the defined boundary.
- Additional top-side mounting hole locations may be added as needed. The thread specification used in any additional holes should be consistent with the thread specification defined below.
- Suggested mounting hold thread specification: M3.5 x 0.6
- TTP thickness (H2) at the mounting hole locations should be a minimum of 3mm to ensure at least 5 threads of engagement.
- Screws on the liquid cooling assembly should not protrude through the TTP spreading surface (H2) in order to not impact component placement under the TTP.
- Additional interface points for mechanical shock/vibration support may be required due to the added weight of the TTP and liquid cooling assembly. For example, additional tapped holes on the TTP for mounting brackets to secure to or within the host chassis.

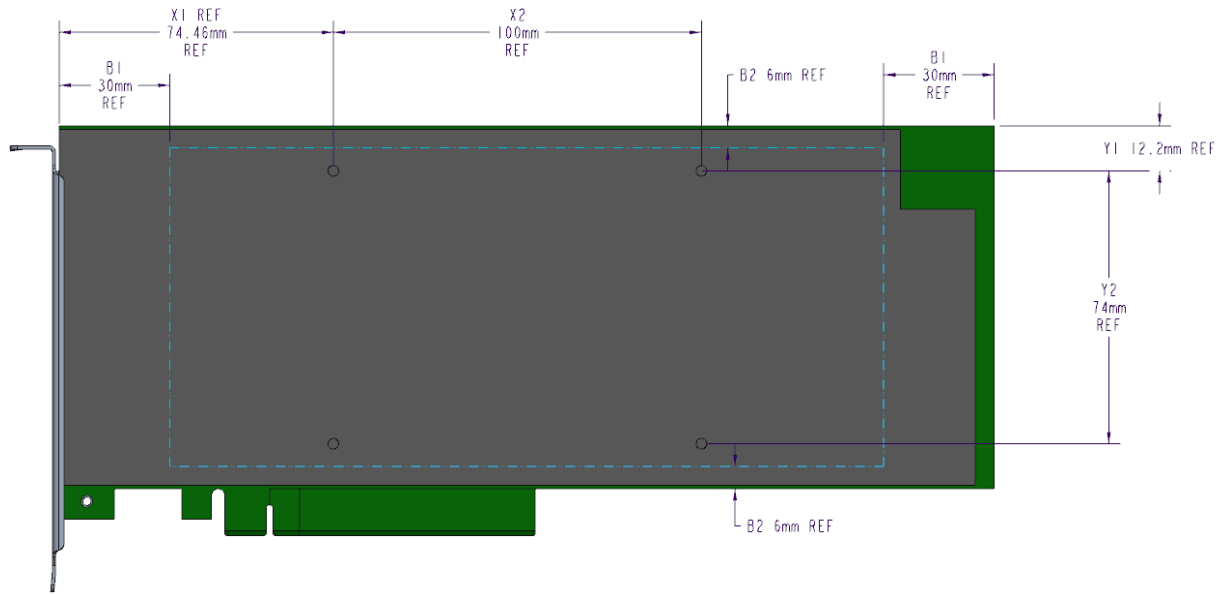


Figure D-14. Example Add-in Card Mounting Hole and Boundary Definition



Appendix E. Acknowledgements

The following persons were instrumental in the development of the *PCI Express Card Electromechanical Specification*:⁷.

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		Cliff Lee	Intel Corporation
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⁷ Company affiliation listed is at the time of specification contributions.

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PT Lim	Molex Incorporated
Jasmine Lin	AMD
Eric Ling	Foxconn Interconnect Technology
Yun Ling	Intel Corporation
Howard Locker	IBM Corporation
Eric Lotter	Cisco/Pure Storage
Grady Maass	IBM Corporation
Alan MacDougall	Molex Incorporated
Bob Marshall	FCI
Bob Martinson	Lotes
Mohiuddin Mazumer	Intel Corporation
Mike Miller	IBM Corporation
Glenn Moore	Foxconn Interconnect Technology
Dave Moss	Dell Technologies
Jay Neer	Molex Incorporated
Manisha Nilange	Intel Corporation
Scott Noble	Intel Corporation
John Norton	NVIDIA
Ta-Wee Ong	Molex Incorporated
Nima Osqueizadeh	AMD
John Pescatore	Dell Technologies
Edmund Poh	Molex Incorporated
Curt Progl	Dell Technologies
Gamal Refai-Ahmed	Xilinx
Eddie Reid	Intel Corporation
Steve Reinhold	Tektronix
Matt Richardson	IBM Corporation
Martha Rupert	FCI
Rodrigo Samper	IBM Corporation
Bill Sauber	Dell Technologies
Joseph Schachner	Teledyne LeCroy
Chris Schmolze	Bellwether Electronics Corporation
Rick Schuckle	Dell Technologies
Joe Sekel	Dell Technologies
Kalev Sepp	Tektronix
Wenjun Shi	NVIDIA
Joanne E. Shipe	Foxconn Interconnect Technology
Dave Sideck	FCI
Bill Simms	NVIDIA

Chuck Stancil	Hewlett-Packard Enterprise Company
John Stuewe	Dell Technologies
Tom Sultzer	FCI
Toru Tamaki	Tyco International, Ltd.
Junichi Tanigawa	Tyco International, Ltd.
Clay Terry	3DLabs, Inc. Ltd.
SY Theng	Molex Incorporated
Alok Tripathi	Intel Corporation
Andy Vasbinder	FCI
Gary Verdun	Dell Technologies
Andy Volk	Intel Corporation
Jim Waschura	Tektronix
Clint Walker	Intel Corporation
Marc Wells	Intel Corporation
Timothy Wig	Intel Corporation
Zachary Wilhoit	NI
Chris Womack	Hewlett-Packard Enterprise Company
Mike Woren	Tyco International, Ltd.
Yoshisha Yamamoto	Tyco International, Ltd.
Pat Young	Luxshare-ICT
Dave Zenz	Dell Technologies
Lin Zhang	AMD